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Heat distribution simulation and visualization with fast response for power modules

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Abstract: A commonly used simulation method for heat distribution within the power module is the 3D FEM analysis. After the meshing of the solid model of the power module, entering power stimulus values and launching the simulation the heat distribution can be obtained. However the excitation signals are highly dependent on the application parameters describing Vdc, Iout, Vout, cosphi, fsw, etc. If an application parameter is changed the simulation must be run again, which can take a relatively long time for a full analyses. An alternative method is described below, that uses the linearity and superposition property of the heat equation for a quasi real time solution of the heat distribution problem.

1. The heat removal problem:

The life time of power modules is inversely proportional to the operating temperature of the semiconductors. The semiconductors should work at possible lowest temperature in the given application to minimize the power losses and thus the size of the required cooling equipment.
The semiconductors produce heat during operation that increases the temperature of the semiconductor chip and have an influance on the operating temperature of the other semiconductor chips placed near them as well. This is called heat coupling. In case of dense layout the coupled thermal resistance can be significant. It is difficult to measure the exact value of heat coupling between chips however it is easy to calculate using 3D finite element simulation softwares.

2. The heat equation solution:

The heat distribution can be defined with a partial differential equation which describes the distribution of heat (or variation in temperature) in a given region over time.

$$\frac{\partial T}{\partial t} = \alpha\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) + \frac{1}{c_p \rho} q$$

where:

α - thermal diffusivity

$\frac{\partial T}{\partial t}$ - derivate of the temperature

$\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right)$ - Laplace operator (divergence of the gradient)

$\frac{1}{c_p \rho} q$ - heat source

From the equation arises the linear dependency between the heat source and the temperature rise:

$$q \rightarrow dT$$
$$2 * q \rightarrow 2 * dT$$

That is two times more heat will result in two times higher temperature rise.
And the superposition of two heat sources:

$$q_1 \rightarrow dT_1$$
$$q_2 \rightarrow dT_2$$
$$q_1 + q_2 \rightarrow dT_1 + dT_2$$

That is the temperature rise generated by two heat sources is equal to the sum of the temperature rises generated by each heat source separately.

It is possible to modulate the temperature rise distribution caused by each heat source linearly with the actual power loss and finally superposition the temperature rises caused by all chips to get the total temperature rise distribution.

3. Getting temperature distribution and thermal resistance (Rth) values from 3D FEM simulation:

Let us take a three level MNPC inverter, M260 as an example to show the procedure (fig.1).

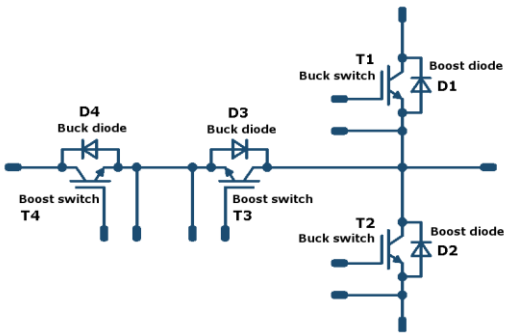

fig.1 – M260 schematic

This module implements four different component electrical functions.

- 2x buck switch (1200V; 2x40A chips paralleled)
- 2x buck diode (600V; 75A)
- 2x boost switch (600V; 75A)
- 2x boost diode (1200V; 50A)

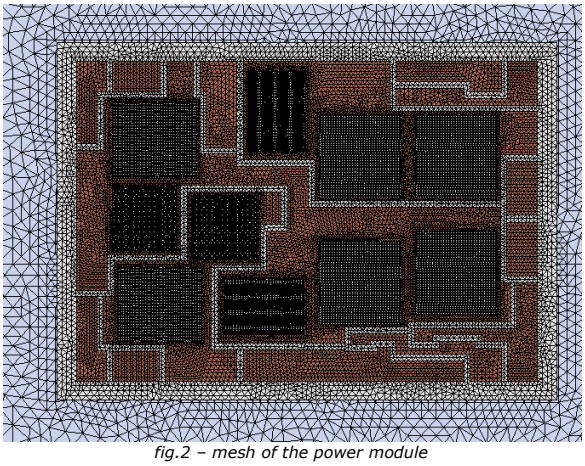

fig.2 – mesh of the power module

The following steps need to be done to get the heat distribution within the module:

- Importing the modul layout into 3D FEM simulator
- Creating the mesh (fig.2)
- Exciting the chips of the same electrical functions by the same load conditions with unity power (1W)
- Running one simulation for each function separately
- Get maximum temperature to define Rth of chip and the temperature distribution (fig.3)

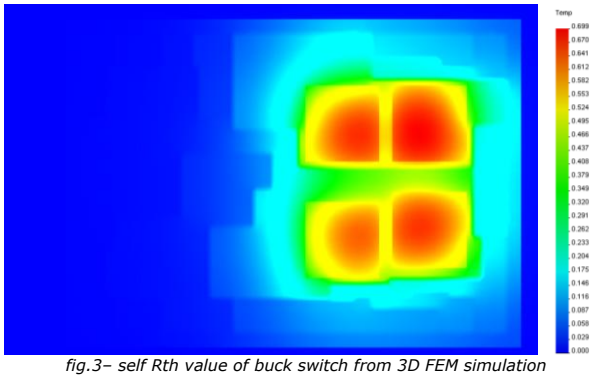

fig.3– self Rth value of buck switch from 3D FEM simulation

The coordinates of maximum heated points can be obtained separately for the different electrical functions and the values define the self Rth values in the heat coupling thermal resistance matrix (diagonal).

$$\begin{bmatrix} 0{,}699 & R_{th_{buckSW-buckD}} & R_{th_{buckSW-boostSW}} & R_{th_{buckSW-boostD}} \\ R_{th_{buckD-buckSW}} & 0{,}1585 & R_{th_{buckD-boostSW}} & R_{th_{buckD-boostD}} \\ R_{th_{boostSW-buckSW}} & R_{th_{boostSW-buckD}} & 0{,}127 & R_{th_{boostSW-boostD}} \\ R_{th_{boostD-buckSW}} & R_{th_{boostD-buckD}} & R_{th_{boostD-boostSW}} & 0{,}1331 \end{bmatrix}$$

fig.4 – self Rth in the matrix

The remaining values (coupled Rths) in the Rth matrix describes the measure how the components heat each other.

4. <u>Defining cross-coupled Rths</u>

Knowing all the chip positions and the temperature rise caused by the neighboring chips the coupled Rth values can be also gained by reading color codes of the different positions for all electrical functions (fig.5)
The black crosses indicate the coordinates of the virtual maximum temperature points.

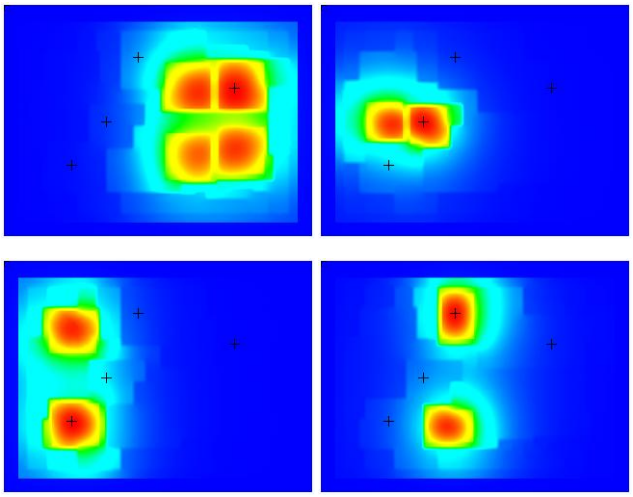

fig.5 - maximum points for different electrical functions

The Rth matrix gives an easy and fast way for calculating each chip temperature of the power module under any load condition.

$$\begin{bmatrix} T_{j_{buckSW}} \\ T_{j_{buckD}} \\ T_{j_{boostSW}} \\ T_{j_{boostD}} \end{bmatrix} =$$

$$\begin{bmatrix} 0{,}699 & 0{,}0393 & 0{,}0087 & 0{,}1179 \\ 0{,}0099 & 1{,}585 & 0{,}3269 & 0{,}0693 \\ 0{,}007 & 0{,}2676 & 1{,}127 & 0{,}0704 \\ 0{,}0415 & 0{,}183 & 0{,}1081 & 1{,}331 \end{bmatrix} * \begin{bmatrix} P_{buckSW} \\ P_{buckD} \\ P_{boostSW} \\ P_{boostD} \end{bmatrix} + \begin{bmatrix} T_{sink} \\ T_{sink} \\ T_{sink} \\ T_{sink} \end{bmatrix}$$

fig.6 – self (black) and cross-coupled (red) Rth matrix

Additionally by superimposing the temperature distributions caused by all functional components the total temperature distribution within the module is obtainable.

The heating power for each function types is obtained from flowTHERM-M260 simulation launched with given application parameters (fig.7).

Vin:	700 V	Vph:	240 V	cos phi:	0,85	Rgon:	4,0 Ohm
Vdc1:	350 V	Iout:	90,0 A	fsw:	20,0 kHz	Rgoff:	4,0 Ohm
fb:	50,0 kHz	C:	1500 uF	fout:	50 Hz	Vgon:	15,0 V
				mod.:	normal	Vgoff:	-15,0 V

Tsink = 80,0 °C

fig.7 – application parameters

Heat powers for the specific application case (Fig.8)

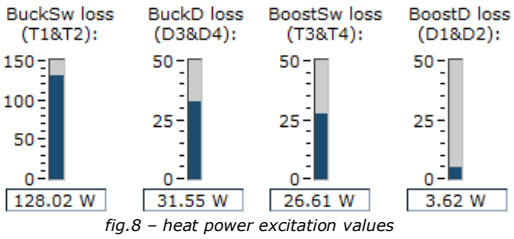

fig.8 – heat power excitation values

The temperature values for the functions are determined by substituting the heat power excitation values.(Fig.9)

$$\begin{bmatrix} T_{j_{buckSW}} \\ T_{j_{buckD}} \\ T_{j_{boostSW}} \\ T_{j_{boostD}} \end{bmatrix} = \begin{bmatrix} 0{,}699 & 0{,}0393 & 0{,}0087 & 0{,}1179 \\ 0{,}0099 & 1{,}585 & 0{,}3269 & 0{,}0693 \\ 0{,}007 & 0{,}2676 & 1{,}127 & 0{,}0704 \\ 0{,}0415 & 0{,}183 & 0{,}1081 & 1{,}331 \end{bmatrix} * \begin{bmatrix} 128{,}02 \\ 31{,}55 \\ 26{,}61 \\ 3{,}62 \end{bmatrix} + \begin{bmatrix} 80 \\ 80 \\ 80 \\ 80 \end{bmatrix}$$

fig.9 – full matrix equation

By the superposition of all distribution layers caused by the functional components the total distribution can be gained.(Fig.10)

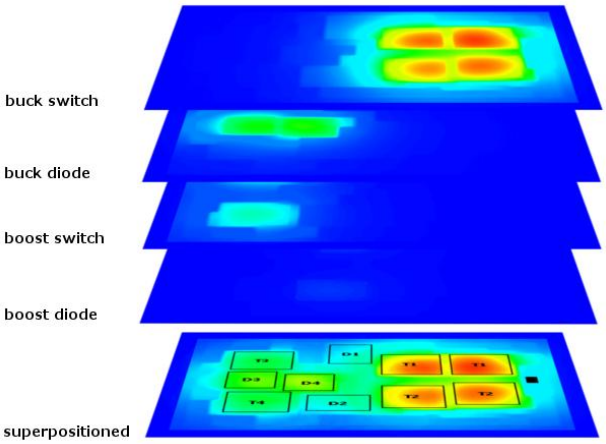

fig.10 - layered and superpositioned thermal distributions

In the final distribution the colors are normalized to the T_{sink} heatsink (min) and to the allowed T_j maximal chip temperature (max) as shown on Fig.11.

hue=0
sat=240
lum=240

hue=160
sat=240
lum=240

$T_{jmax_{tot}}$ (max) T_{sink} (min)

fig11 – define linear color range

Thus each pixel temperature of the superpositioned picture can be read by a resolution of 1/160 due to the hue=0 ($T_{jmax_{tot}}$) and hue=160 (T_{sink}) range.

Conclusion:

An alternative method as described above, which uses the linearity and superposition property of the heat equation, allows building power module loss and temperature simulators with very fast response to adjustments or changes in the application parameters.
The simulation tool can easily be programmed to map the relations between virtual junction temperature of semiconductor chips inside the power module and a temperature sensing device. (Fig 12.)
This information used in a real time temperature calculation of the application can be used for an accurate estimation of the virtual chip temperatures.
As next steps the visualization of the fluctuation of the chip temperatures with the converters basic frequency is to be solved.

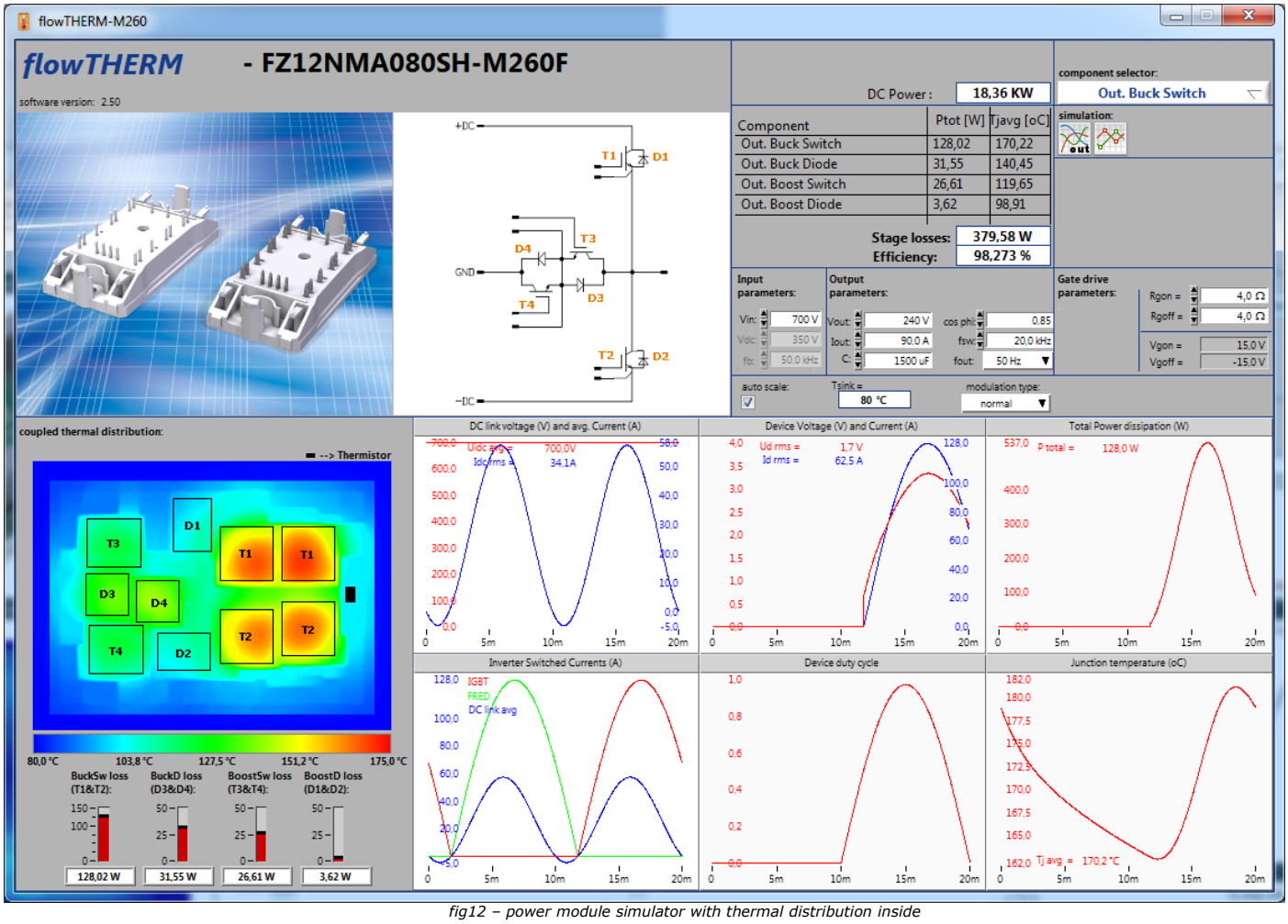

fig12 – power module simulator with thermal distribution inside