Innovative Topologies for High Efficient Solar Applications

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With the race towards highest efficiency innovative topologies are more often considered for the development of new power conversion products. Old well known ideas revive because the advanced power module technology in connection with elevated requirements into efficiency makes the utilization economical. In the following are power module topologies with paralleled MOS-FET – IGBT switch presented dedicated for new high efficient solar applications.

Parallel Switched MOS-FET with IGBT

The combination addresses two basic improvements in efficiency:

1. Boosting of efficiency at the high load range by rendering the static losses of the switch to the IGBT and the dynamic losses to the MOS-FET.
2. Boosting of efficiency at light load range by rendering both the static and the switching losses to the MOS-FET.

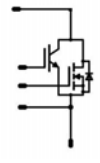

Fig. 1: MOS-FET parallel with IGBT

The MOS-FET turns on fast and is delayed at switch off so that the switching losses are assigned to the MOS-FET. The MOS-FET will also carry the current at low power so eliminating one pn junction voltage drop of the IGBT whereas the IGBT will take the majority at max load condition. At low load the IGBT is not conducting at all so residential tail current losses are eliminated for the whole power range. With this topology it is possible to improve both the overall and the maximum load efficiency.

Gate Control

At switch on the Gate of the MOS-FET is direct paralleled with the IGBT gate because the MOS-FET will be faster and take over the switch on losses. But at switch off, the MOS-FET has to be delayed to release the IGBT from switch off losses. For this timing there are different possibilities available:

1. Separate gate signal by two drivers.
The independent access to both gates offers the maximum flexibility and optimal results are achievable. Delaying the turn off drive signal to the MOS-FET exploits the maximum advantages of the switch.

2. Separate gate signal by single driver:
The following simple circuit resulted in maximum performance.

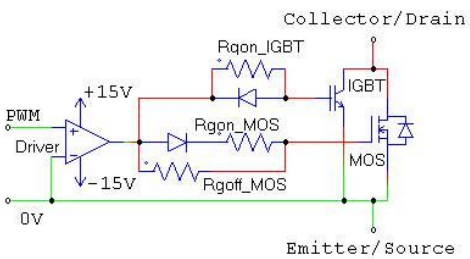

Fig. 2: driver with separate gate access

3. Single gate connection:
For power modules, it is an advantage to offer pin compatible solutions with standard switches. In that case there are additional gate pins resulting in a disadvantage. This approach is supported by the following gate control topology:

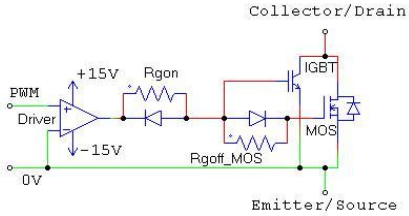

Fig. 3: driver for single gate connection

The gate resistance for the MOS-FET is included in the power module. The dynamic behavior is only minimal worse compared with the separate gate circuit.

4. Direct connected:
It is also possible to connect the gates directly. Here are two remaining possibilities. With a standard gate driver circuit we will reduce only the switch on losses, which will reduce already the total dynamic losses significantly. But it is also possible to generate a 3 level gate signal and to use an IGBT with higher threshold voltage. The IGBT will already switch off at the 2nd level voltage whereas the MOS-FET will take over the current before switching off with 0V gate voltage. The draw back of this idea is the relative high tolerances of the threshold voltages.

Ideas for New Topologies

The parallel idea could be used in all IGBT based topologies were the switching losses are significant high and in every MOS-FET topologies with significant static losses. For solar applications especially the following topologies might be of interest:

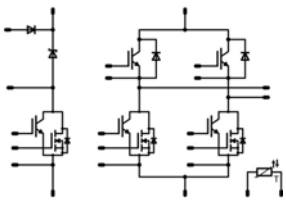

Fig. 4: booster + mixed inverter bridge

NPC topologies will play a significant role for applications with power ratings > 7kW and DC voltages higher than 600V. One example is the

following topology which is available as an integrated power module:

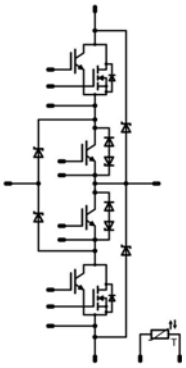

Fig. 5: NPC topology as integrated in the P969-F power module

Utilization of 1200V diodes will transport the reactive current because the intrinsic characteristics of the diodes of the MOS_FET´s are disabled. The suppresser diode connected with a high voltage FRED protects the IGBT from reverse current when the parasitic capacity of the MOS-FET is charged at switch off.
In the following the module P965-F - 45mΩ - CoolMOS™ (solid line) is compared with the P969-F using a 99mΩ CoolMOS™ in parallel with an PT-IGBT(dashed line). f=16kHz, P_N = 10kW

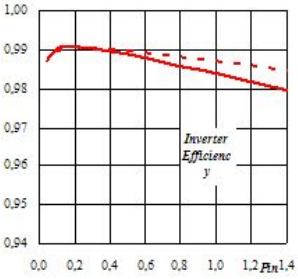

Fig. 6: efficiency comparison: mixed NPC (solid) vs. mixed, paralleled NPC (dashed)

The following 3 level inverter topology is able to gain further efficiency with the usage of higher voltage switches:

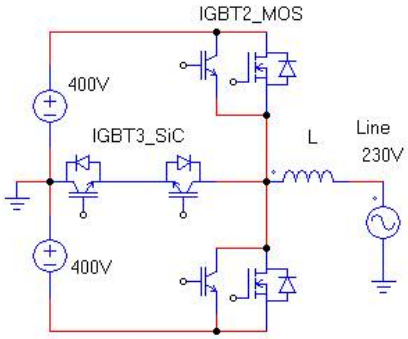

Fig. 7: high voltage NPC

With this circuit efficiency > 99% is reachable at higher power levels. Because of the neutral clamping, it is possible to use the MOS-FET up to nearly the brake down voltage. The handling of reactive power is limited due to the limitation of the body diode of the MOS-FET. To cover this approach, the following circuit is the recommended alternative:

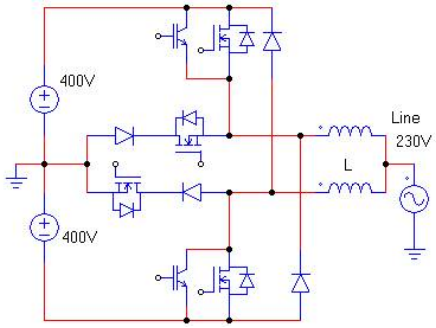

Fig. 8: high voltage NPC with reactive load capability

The switch in the neutral point clamp could be either a MOS-FET or an IGBT or both.

Conclusion

With the paralleling of MOS-FET and IGBT, it is possible to achieve a nearly constant efficiency at the highest level. The exploitation of this well known paralleling technology was hindered by the complexity of semiconductor technology selection criteria, gate drive technologies, and the dependency of the results on layout causing parasitic stray inductances of discrete devices. With an advanced power module technology, the utilization now more than economical. The power modules which are supporting this idea are available as a standard product or they can be defined as customized components. The future approach of reactive power capabilities is already incorporated.

References

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