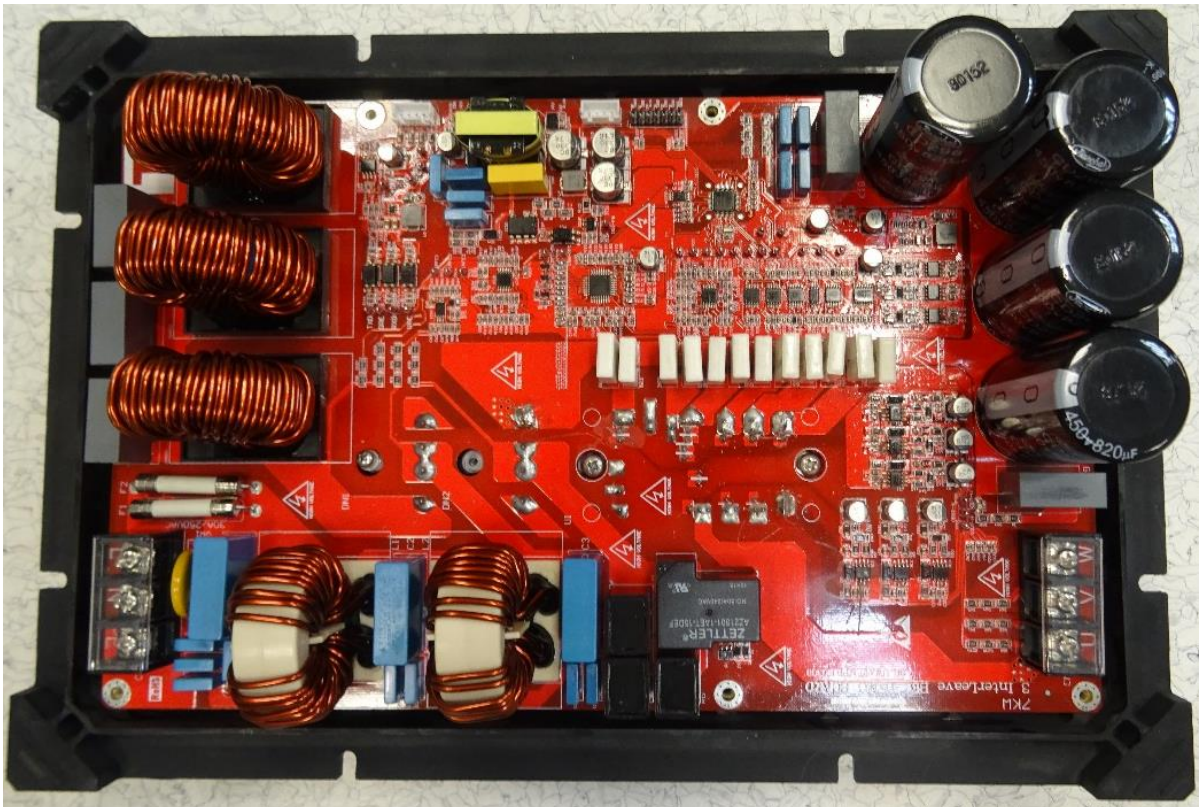
Vincotech

Reference Design for flowPIM 1 + PFC Modules

Evaluation Board



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Revision History

Date	Revision Level	Description	Page Number(s)
2019.12.18	1	First release	63
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Safety Information

The board described is an evaluation board (EVA board) dedicated for laboratory environment only.
It operates at high voltages. This board must be operated by qualified and skilled personnel familiar with all applicable safety standards.
This EVA board can endanger life by exposure to rotating machinery and high voltages.
The ground potential of the EVA board is not floating it is biased to the negative DC-Link voltage potential. In order to be able to measure by non-floating instrument (oscilloscope) use isolation transformer at the AC input.
Allow at least 2 minutes for the DC-Link capacitor to discharge to safe voltage levels (< 50 V).

Failure to follow these guidelines result personal injury or death and/or equipment damage.

1 Abstract

This application note is intended to demonstrate the performances of the Vincotech *flow*PIM 1 + PFC modules in *flow* 1 housing.

The targeted market for the new topology is the air conditioner application for example: fans, pumps, compressors.

As the power module is not equipped with an input rectifier, the intended application can decide to use one or three-phase rectification. It is even possible to use a common rectifier instead of separate rectifiers for each motor inverter. The PFC booster has three legs which can be used in parallel or interleaved configuration for smaller ripple and inductor size. Integrated capacitors decrease the loop inductance thus enabling even higher switching frequencies. The three-phase inverter uses new generation high-speed 600 V IGBTs. An integrated NTC provides accurate temperature measurements of the power stage. The power module has reduced ceramic thickness for better thermal performance. For the different power levels different rated power modules are available. With the different semiconductor choices a component level multisource is possible.

- Features of ***flow*PIM + PFC** topology:
  - Three-leg interleaved PFC with High-Speed IGBT
  - Three-phase inverter
  - Thermistor

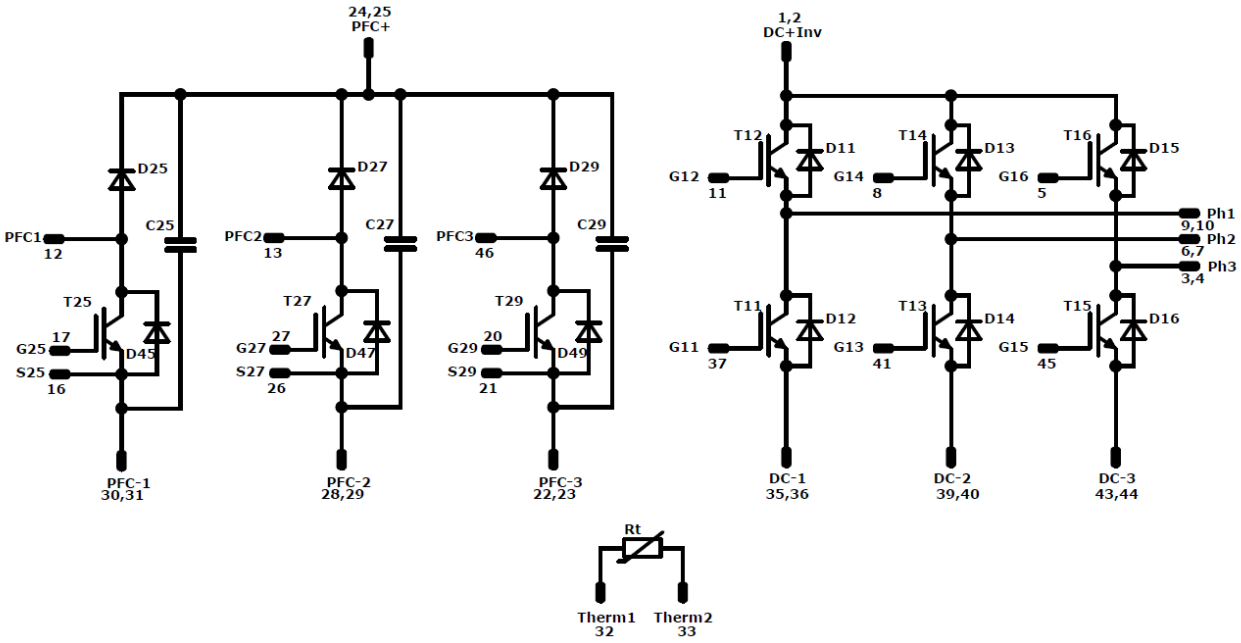
- Features of ***flow* 1** housing
  - Convex shaped substrate for superior thermal contact
  - Thermo-mechanical push-and-pull force relief
  - 0.38 mm ceramic
  - Reliable cold welding connection to PCB
  - Convex shaped baseplate for superior thermal contact

For more information about Vincotech modules please visit www.vincotech.com. This board provides a plug and play solution identifying the switching behavior and efficiency of this module family.

2 Introduction to LH9*-E08T family

Members of the family: Table 1:

Part.-No.	Voltage	Current	Technology
10-PG06PPA050SJ02-LH94E08T	600 V	50 A	TRENCHSTOP™ PERFORMANCE IGBT3.1 High speed 5 FAST IGBT + Stealth™ Diode
10-PG06PPA030SJ02-LH92E08T	600 V	30 A	TRENCHSTOP™ PERFORMANCE IGBT3.1 High speed 5 FAST IGBT + Stealth™ Diode



General features of the module:

- Highly integrated PIM with interleaved PFC circuit
- High switching frequency PFC circuit
- On-board capacitors
- New generation high speed IGBTs in the inverter

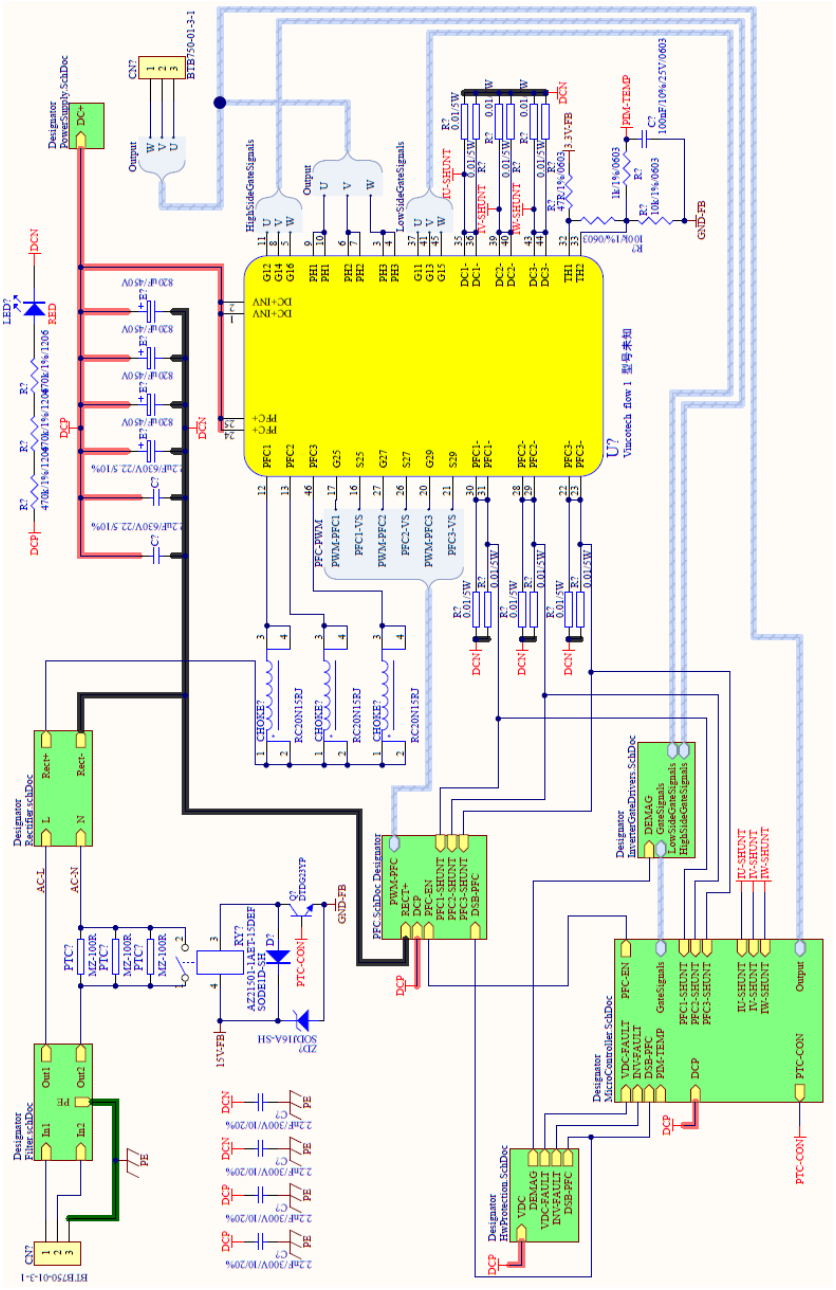
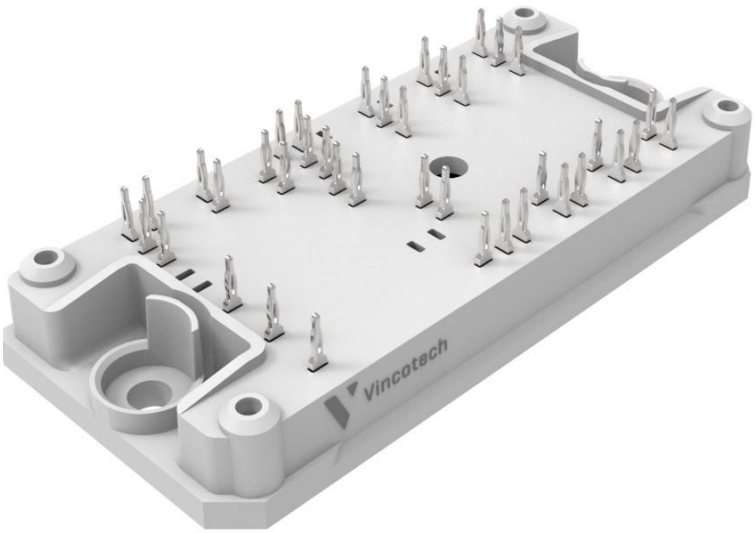
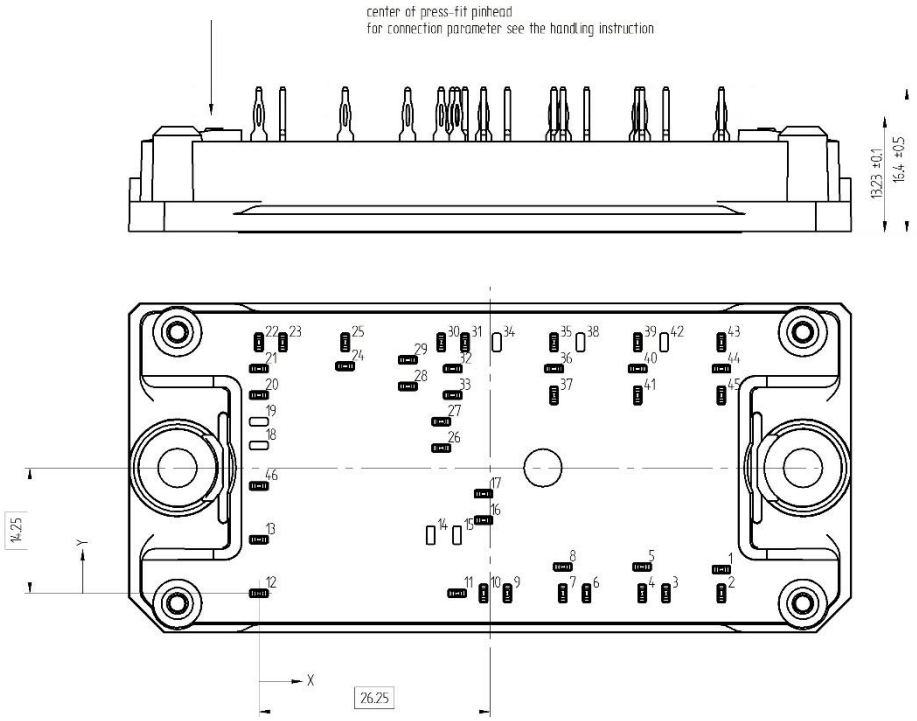


Figure 1: Simplified PFC-INVERTER block diagram

Pin table			
Pin	X	Y	Function
1	52,5	2,7	DC+Inv
2	52,5	0	DC+Inv
3	46,2	0	Ph3
4	43,5	0	Ph3
5	43,5	3	G16
6	37,2	0	Ph2
7	34,5	0	Ph2
8	34,5	3	G14
9	28,2	0	Ph1
10	25,5	0	Ph1
11	22,5	0	G12
12	0	0	PFC1
13	0	6,1	PFC2
14	Not assembled		
15	Not assembled		
16	25,5	8,3	S25
17	25,5	11,3	G25
18	Not assembled		
19	Not assembled		
20	0	22,5	G29
21	0	25,5	S29
22	0	28,5	PFC-3
23	2,7	28,5	PFC-3
24	9,8	25,8	PFC+
25	9,8	28,5	PFC+
26	20,7	16,5	S27
27	20,7	19,5	G27
28	16,9	23,5	PFC-2
29	16,9	26,5	PFC-2
30	20,7	28,5	PFC-1
31	23,4	28,5	PFC-1
32	22	25,5	Therm1
33	22	22,5	Therm2
34	Not assembled		
35	33,5	28,5	DC-1
36	33,5	25,5	DC-1
37	33,5	22,5	G11
38	Not assembled		
39	43	28,5	DC-2
40	43	25,5	DC-2
41	43	22,5	G13
42	Not assembled		
43	52,5	28,5	DC-3
44	52,5	25,5	DC-3
45	52,5	22,5	G15
46	0	12,2	PFC3

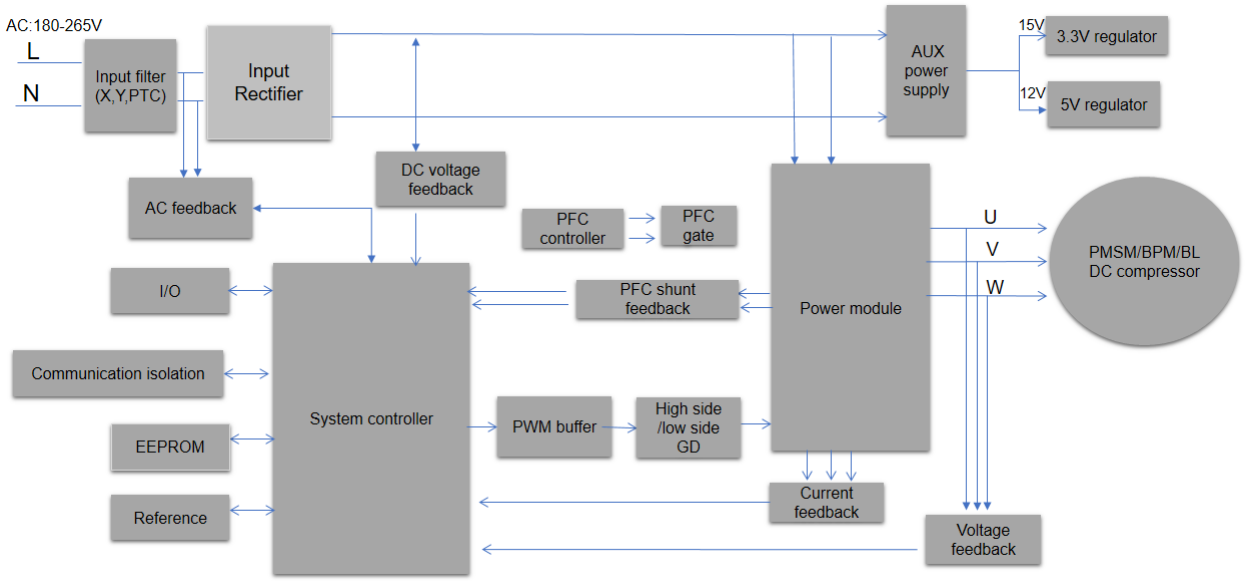




3 Introduction of the EVA board

The evaluation board includes the power supply electronics of a typical air conditioning unit. From the single phase input to the variable frequency output functional and safety aspects are implemented. After the input filter and rectification an industry standard PFC controller IC is responsible for the clean power factor at the input. The FAN9673 is a 3 channel interleaved continuous conduction mode (CCM) controller for boost type power factor correction. The channel management is disabled, output frequency is set to 40 kHz and output voltage to 385 V. Under voltage, brownout, current limit functions are operational. The output inverter control is realized with Texas Instrument's C2000 family 32-bit Piccolo™ Microcontroller. The C2000 family is intended for real time digital signal processing for motor drives among others. For more information on the utilized parts please visit the manufacturer's website. The output voltage and current of each phase is monitored and regulated by the control loop.

The main controller is also monitoring the status of the whole device. The power module's temperature, PFC currents, input, DC-link voltage and fault status is monitored.



- Single-phase 180 V_{AC} – 265 V_{AC} input voltage
- Onboard EMI filter, fuse, PTC inrush protection
- Complete solution for a 5 kW to 7 kW 3 phase motor drive application
- Discrete CCM PFC controller (no software needed)
- Adjustable motor parameters and speed
- On board auxiliary power supply for logic and protection
- Isolated RS485 communication with MODBUS protocol
- Labeled test points for easy evaluation and debugging
- Demagnetization, DC-link over voltage, gate under voltage protection and current limit

4 Design goals

This application note illustrates the design process and component selection for a continuous current mode power factor correction boost converter utilizing the FAN9673.

The three-phase inverter is controlled by TI's C2000 MCU and driven by FAN73711MX gate drivers. For the power stages the Vincotech's **10-PG06PPA050SJ02-LH94E08T** power module is used.

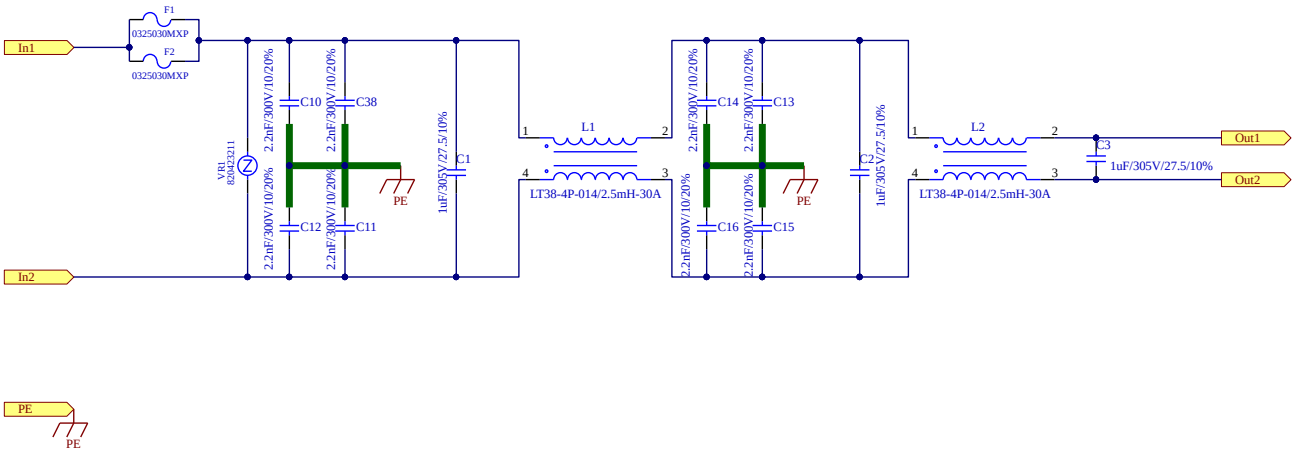
Table 2: Technical specification

Parameter	*Symbol*	*Test condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Remarks*
PFC Characteristics							
AC input voltage	$V_{AC,IN}$		180	220	265	V_{RMS}	f_{in}=47-63 Hz
Input frequency	f_{LINE}		47		63	Hz	
DC-Link voltage	V_{DC}			385		V_{DC}	
PFC switching frequency	$f_{SW,PFC}$	$f_{SW,PFC}$		40		kHz	
Inverter Characteristics							
Inverter AC output voltage	$V_{OUT,AC}$			220		V_{AC}	385V DC-Link SPWM modulation
AC output current	$I_{OUT,AC}$	$V_{AC,IN} \geq V_{AC,IN(Typ)}$	-55		55	A_{pk}	

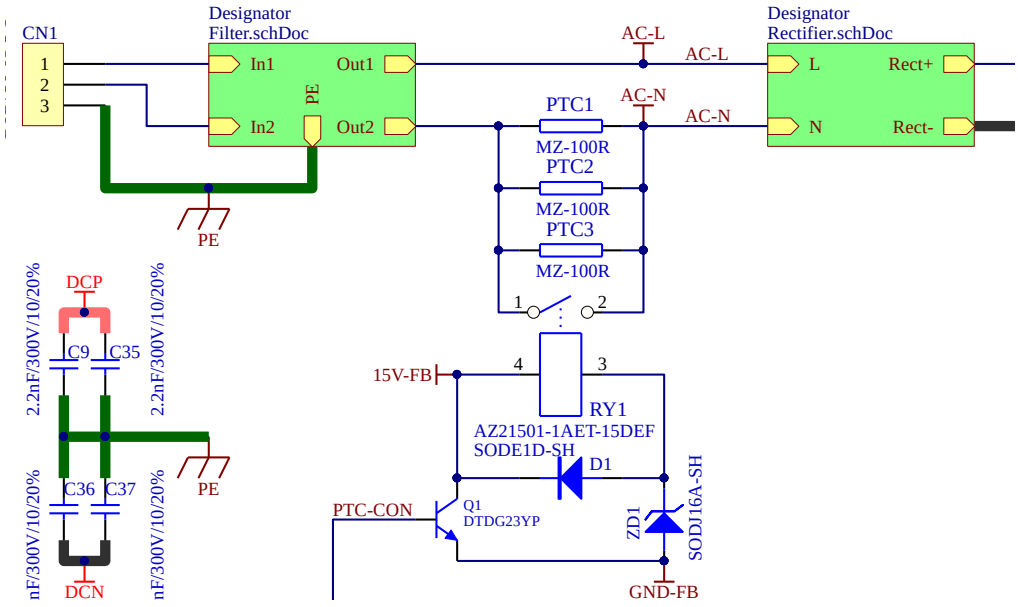
5 Circuit description

5.1 Line input

The AC line input side comprises the input AC terminals (CN1), fuses (F1, F2) as over-current protection and a varistor (VR1) for over voltage protection. Two stage common and differential mode filtering is done by common mode chokes (L1, L2), X-capacitors (C1, C2 and C3) and Y-capacitors (C38, C10, C11, C12, C13, C14, C15 and C16).



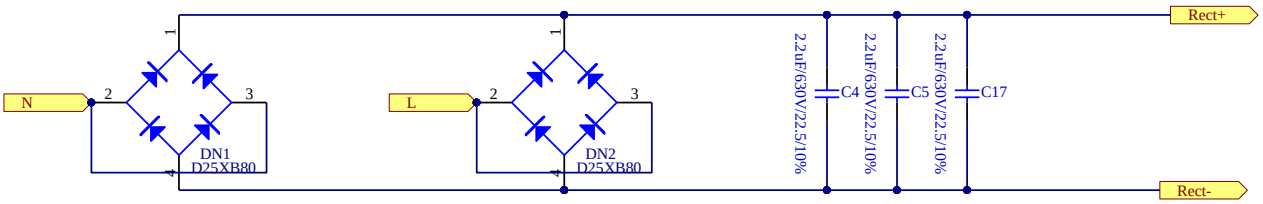
The input inrush current caused by the charging current of the DC link capacitors is limited with PTCs (PTC1, PTC2, and PTC3). If the capacitors are fully charged, the PTCs introduce unwanted losses to the circuit. Therefore, the PTCs are bridged over with relay RY1. The relay is capable to carry the current of the inverter (up to 50 A). The relay's coil operates from 15 V supply. Level shifting is done with an NPN digital transistor (Q1) which is connected to GPIO29.



5.2 Rectifier

The AC input is rectified with a full bridge rectifier. The rectifier is realized with two diode bridge modules (DN1, DN2) connected in parallel. The current rating is doubled from 25 A to

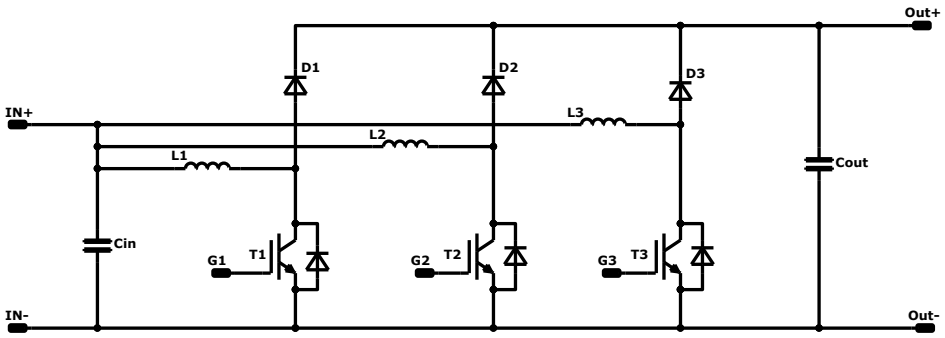
50 A. The output of the rectifier is the input of the boost PFC stage. The output of the rectifier is filtered with capacitors (C4, C5, and C17).



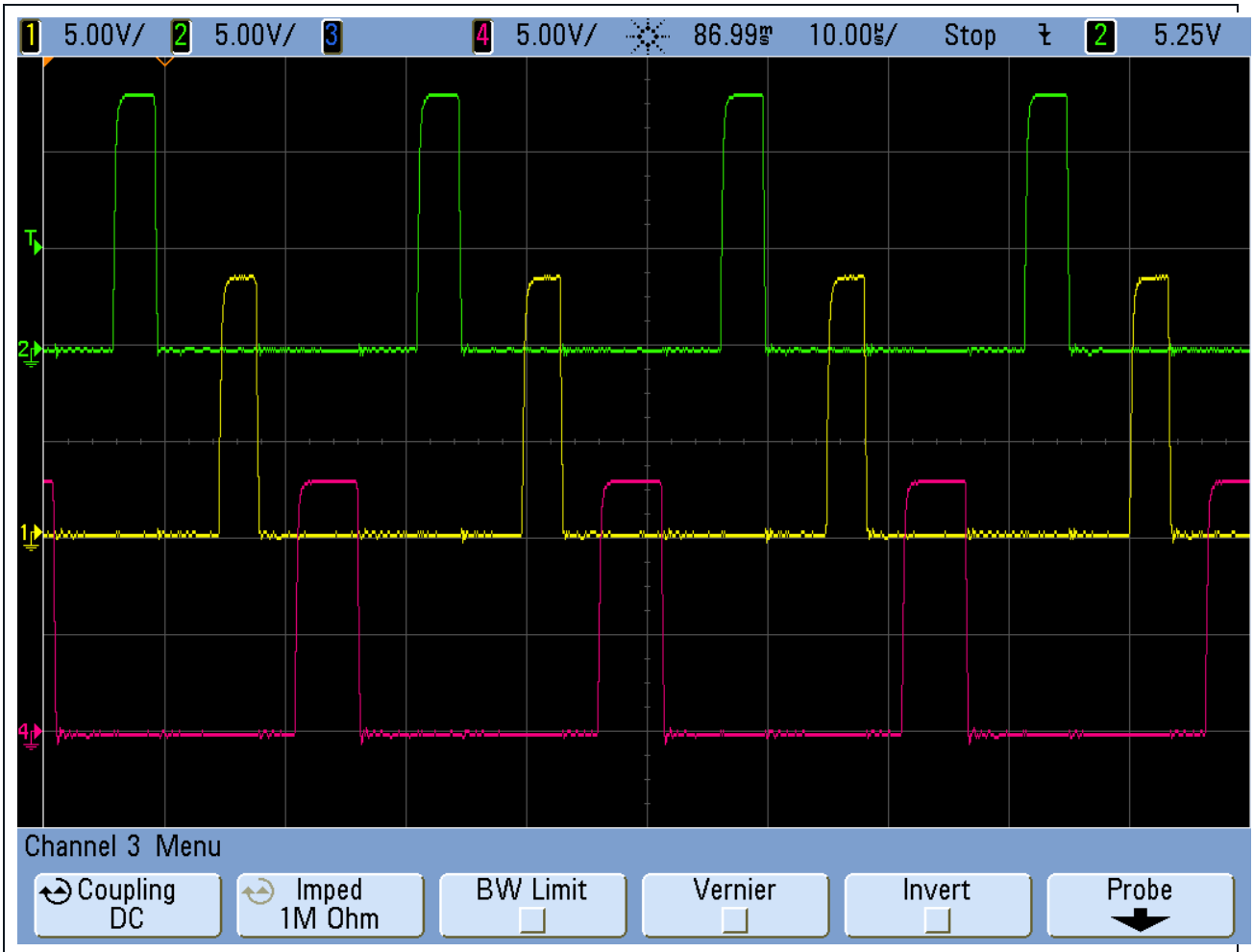
5.3 PFC

5.3.1 Interleaved converters

Interleaved DC-DC switching converters are constructed from multiple instances of paralleled elementary converters (e.g. boost converter). The switch-on/-off events of each converter leg is equally distributed in one switching period. The input and output capacitors are common and each leg has its own inductor.



This arrangement enables much lower RMS current value on the capacitors, lowering the required capacitor size and/or voltage ripple. This configuration results also in better EMI performance thanks to lower ripple and higher frequency. Due to smaller capacitor values the dynamics of the converter can be enhanced.



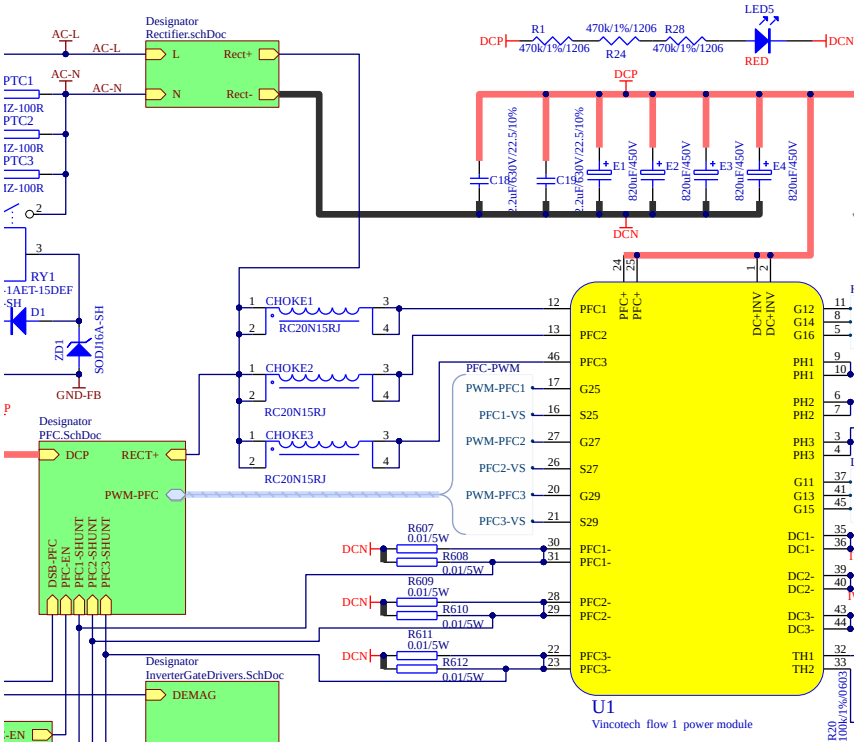
Gate signals of interleaved boost converter

The output power of the converter is distributed on the elementary legs of the interleaved converter. This way the serial elements (inductors, semiconductors) will require lower current capability.

5.3.2 PFC design

PFC is a CCM (continuous conduction mode) boost type interleaved converter. Boost inductors CHOKE1, CHOKE2, CHOKE3, output capacitor C18, C19 (4.4 µF) and DC-link buffer capacitors E1-E4 (3.28 mF). The capacitance is sized to reduce the output voltage ripple

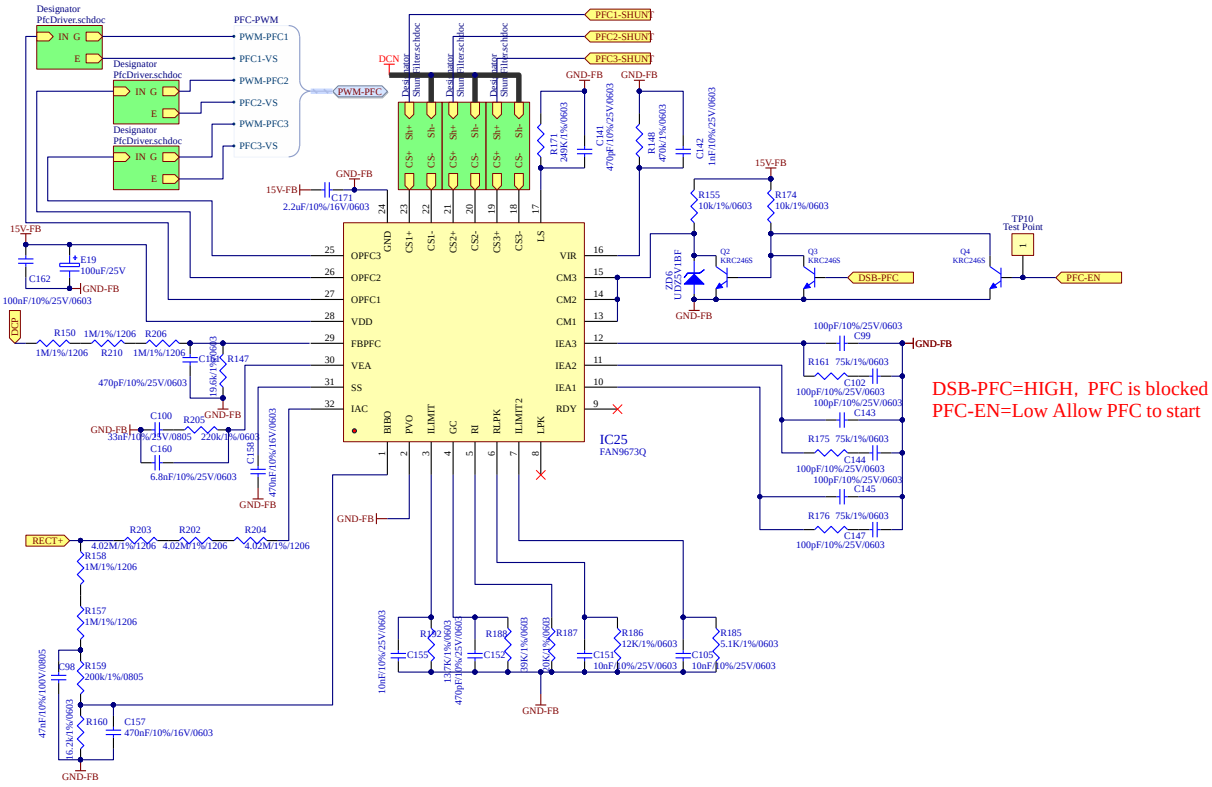
(100Hz) to an acceptable level and to meet the holdup time requirements.



The PWM control of the boost converter is made with FAN9673. This is a three-channel interleaved CCM controller for wide range line input applications from 180 to 265 VAC. The switching frequency is programmed to 40 kHz with R187.

The IC is equipped with various protection features to ensure safe operating condition for both the system and device. The PFC switching frequency can be programmed by R187 and DC-Link voltage with R150, R210, R206, R147, C161 divider network.

Channel management and output voltage programming functions are disabled. The ready-signal is not forwarded to the microcontroller. However, the PFC state can be predicted from the DC-link voltage.



The CM pins are used to disable the operation of the controller. The microcontroller and the hardware over voltage protection circuit can disable the operation of the PFC. The protection trip point is at 440 V (this will be described in the hardware protection section). Q2-Q4 transistors and ZD6 Zener diode with R155, R174 realize an OR gate to combine and level shift the two signals.

The voltage control loop error amplifier is referenced to 2.5 V. The feedback resistor network results in 385 V DC link voltage.

Let

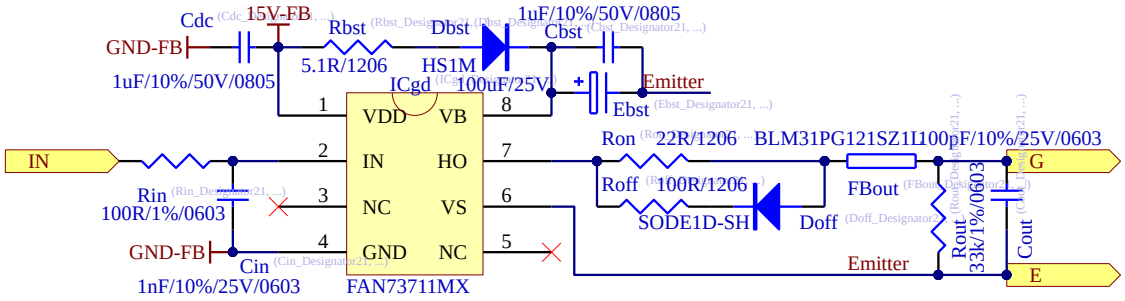
$$R_{in} = R_{147} = 19{,}6k\Omega$$

$$R_{out} = R_{150} + R_{210} + R_{206} = 1M\Omega + 1M\Omega + 1M\Omega = 3M\Omega$$

Then

$$V_{out} = \frac{V_{ref}}{R_{in}}(R_{in} + R_{out}) = \frac{2{,}5V}{19{,}6k}(19{,}6k + 1M + 1M + 1M) = 385V$$

The PFC gate drivers are FAN73711 gate drive ICs with 22 Ω turn-on and 18 Ω turn-off resistance. The driver has high frequency filtering. Since the PFC shunts are connected to the exact same ground as the control, it is necessary to isolate the driver output from the control. The bootstrap circuit decouples the emitter from the ground of the control.

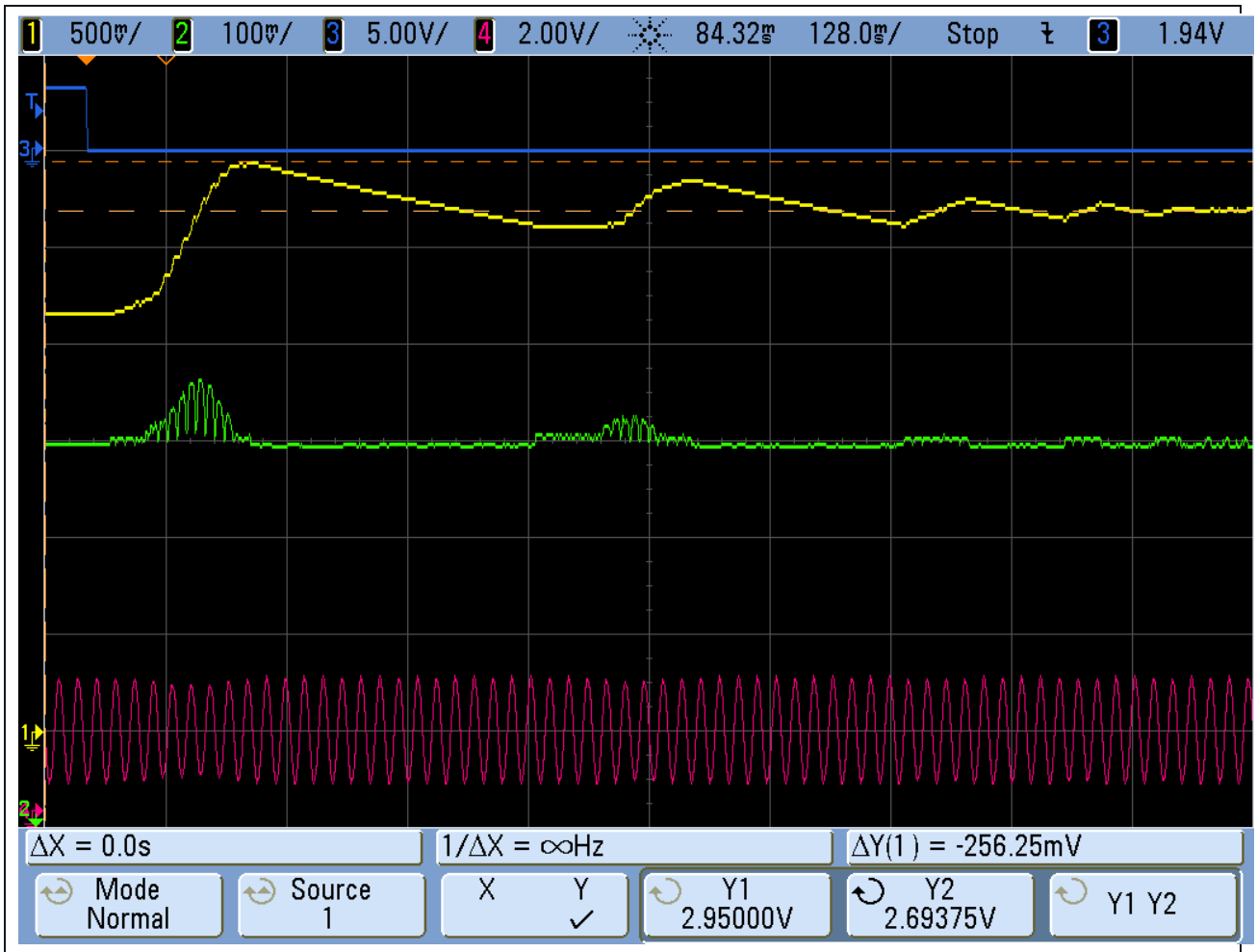


Bootstrap under voltage protection (UVLO) is utilized to avoid desaturation due to insufficient gate voltage. When the bootstrap capacitor's voltage is under 8.3 V (typical) the gate driver will stop operating.

PFC gate and current waveforms

The interleaved gate signals result a phase shifted current waveform. The 2nd channel gate signal (blue) was measured directly with a differential probe 1:10 and the two current waveforms on

their corresponding test point. The current of the measured transistor (green) is rising when the transistor is open, and zero when it is commutated to the boost diode. The output current of the PFC stage is 10 A (3.3 A for each leg). Please note the high noise levels at the test points. This is the result of the large ground loop created by probing the test points in the proximity of the switching components. These points are primarily designed for the debugging of the microcontroller without the high EMI from the power stage.



PFC start-up

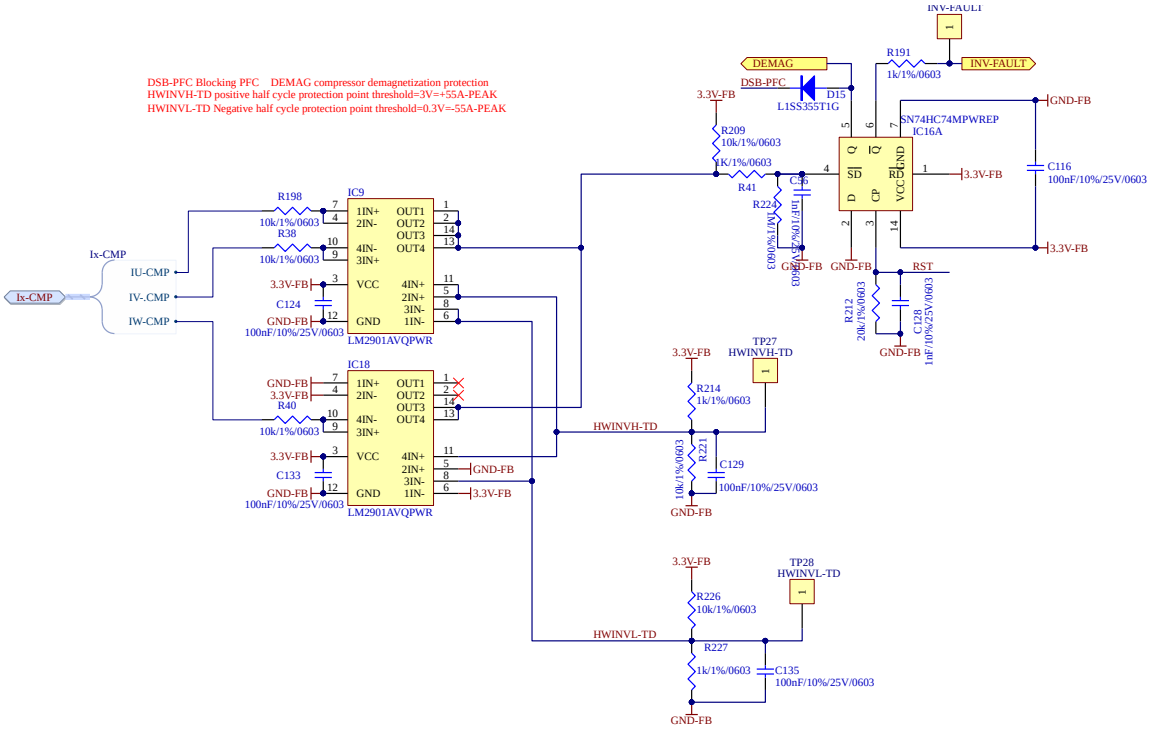
After the system has been connected to the input AC power the DC link voltage (yellow) reaches the peak of the input voltage. After the relay bridges the PTCs the PFC controller can be enabled on PFC-EN (blue). At this time the controller synchronizes with the AC input voltage (purple) and increase the current reference in phase with the input in order to raise the DC link voltage to the desired level. The current can be observed on IPFC1 test point (green). After a slight overshoot (Y1 cursor) the voltage settles at the set voltage (Y2 cursor).

5.4 Protection circuit

The EVA board is equipped with protection circuits such as over-voltage and demagnetization protection. The protection latch stores the fault condition and prevents further operation. The microcontroller can reset the latches on GPIO7.

5.4.1 DEMAG protection

The permanent magnets of a motor exhibits a demagnetizing field whenever current flows in the motor armature. This effect is known as “armature reaction” and will have a negligible effect during normal operation. At high load the magnet saturates and the flux will not rise proportional to the applied field. After this “knee” point of the B-H curve the magnet will not return to its original state i.e. the dipoles change orientation. As a result of this, above a certain level of current, the field magnets will become permanently demagnetized. Therefore, it is important not to exceed the maximum pulse current rating of the motor. This can be achieved by limiting the output current of the inverter. Both the positive and negative current direction are compared (IC9, IC18) with a pre-set level (R214, R221 and R226, R227). If it is exceeded, then the inverter gate drivers are disabled. The comparing voltage levels can be measured on test points HWINVH-TD (TP27) -> 3 V and HWINVL-TD (TP28) -> 0.3 V.



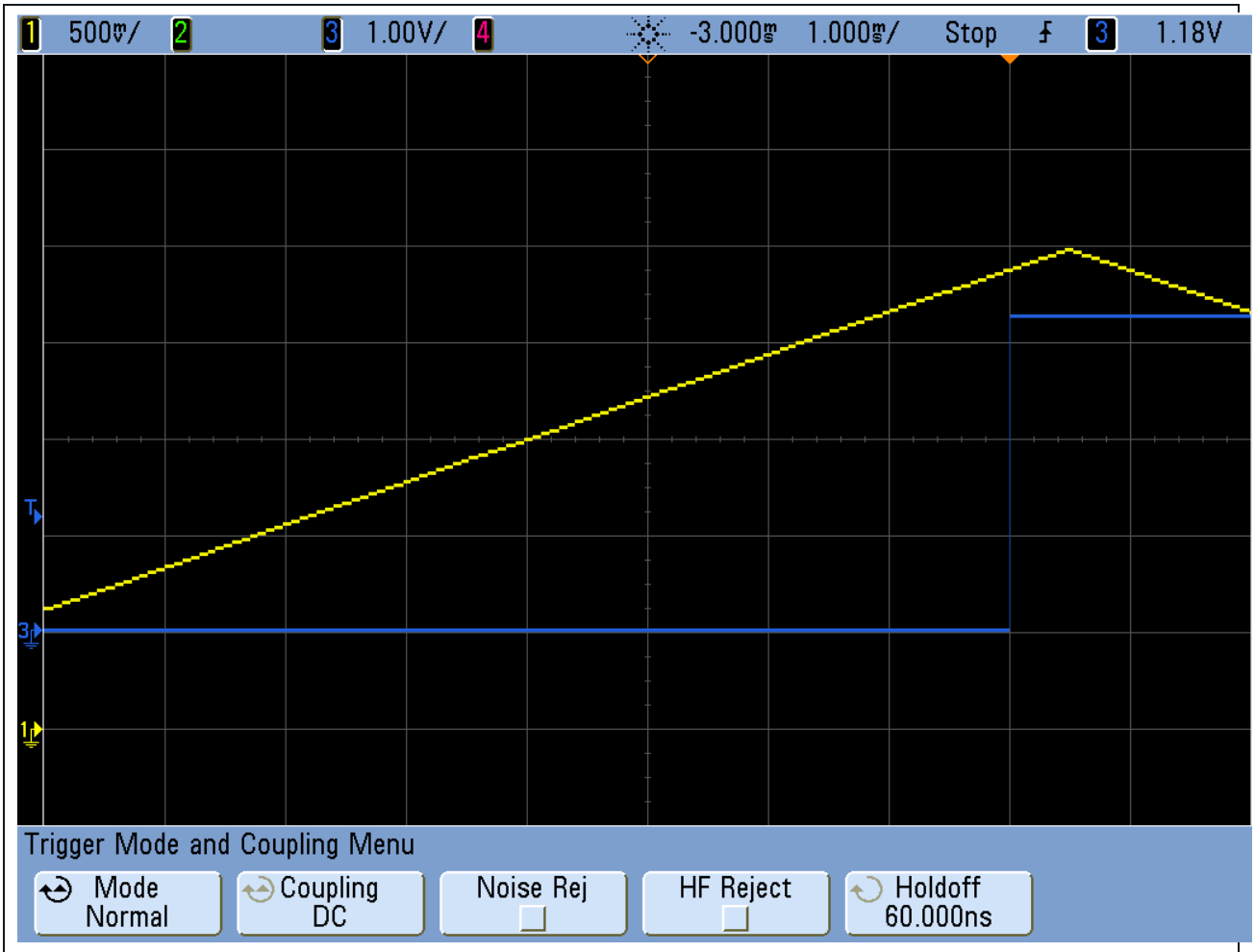
The current transfer ratio is 25 mV/A + 1.65 V (as will be described), therefore the comparator is set to trip at 54 A.

I_{max} can be calculated:

$$3V = 25\frac{mV}{A} \cdot I_{max} + 1{,}65\ \mathrm{V}$$

$$I_{max} = \frac{3V - 1{,}65\ \mathrm{V}}{25\frac{mV}{A}} = 54A$$

The fault latch (IC16) output can be observed on test point DEMAG (TP21), negated output on test point INV-FAULT (TP19). The later signal also can be processed in the microcontroller in GPIO28.



Over current protection trip

When the simulated over current input (yellow) reaches the threshold, the demagnetization protection output (blue) is triggered and holds the error until the RST signal clears the flip-flop's content.

5.4.2 DC-link over voltage protection

On the output of the PFC stage there are several electrolytic capacitors. The voltage rating of them is 450 V, which must not be exceeded under any condition. The Power module's switching transitions also create voltage overshoot; depending on various parameters (switched current, transition speed, temperature etc.). The overshoot is added on top of the DC link voltage.

For safety measure an over voltage protection circuit is added. Consisting of a hysteresis comparator (IC12) and a latch (IC17). The comparator output is at HIGH level if the DC link voltage exceeds 440V (3.1V on the input) and unless the voltage drops below 400V at the DC link (2.83V at the input).

The comparison levels are:

$$V_L = \frac{R_{87} \times R_{77}}{R_{76} + R_{87} \times R_{77}} V_{cc} = \frac{15k \times 10k}{1k + 15k \times 10k} 3{,}3V = 2{,}83V$$

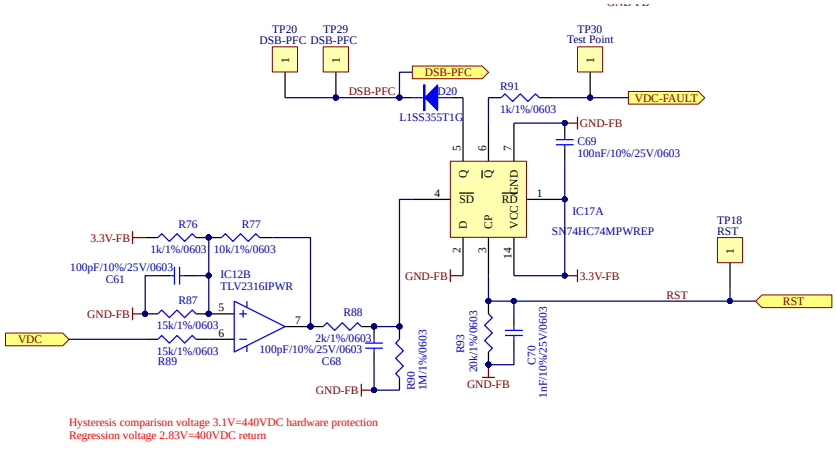
$$V_H = \frac{R_{87}}{R_{87} + R_{76} \times R_{77}} V_{cc} = \frac{15k}{15k + 1k \times 10k} 3{,}3V = 3{,}11V$$

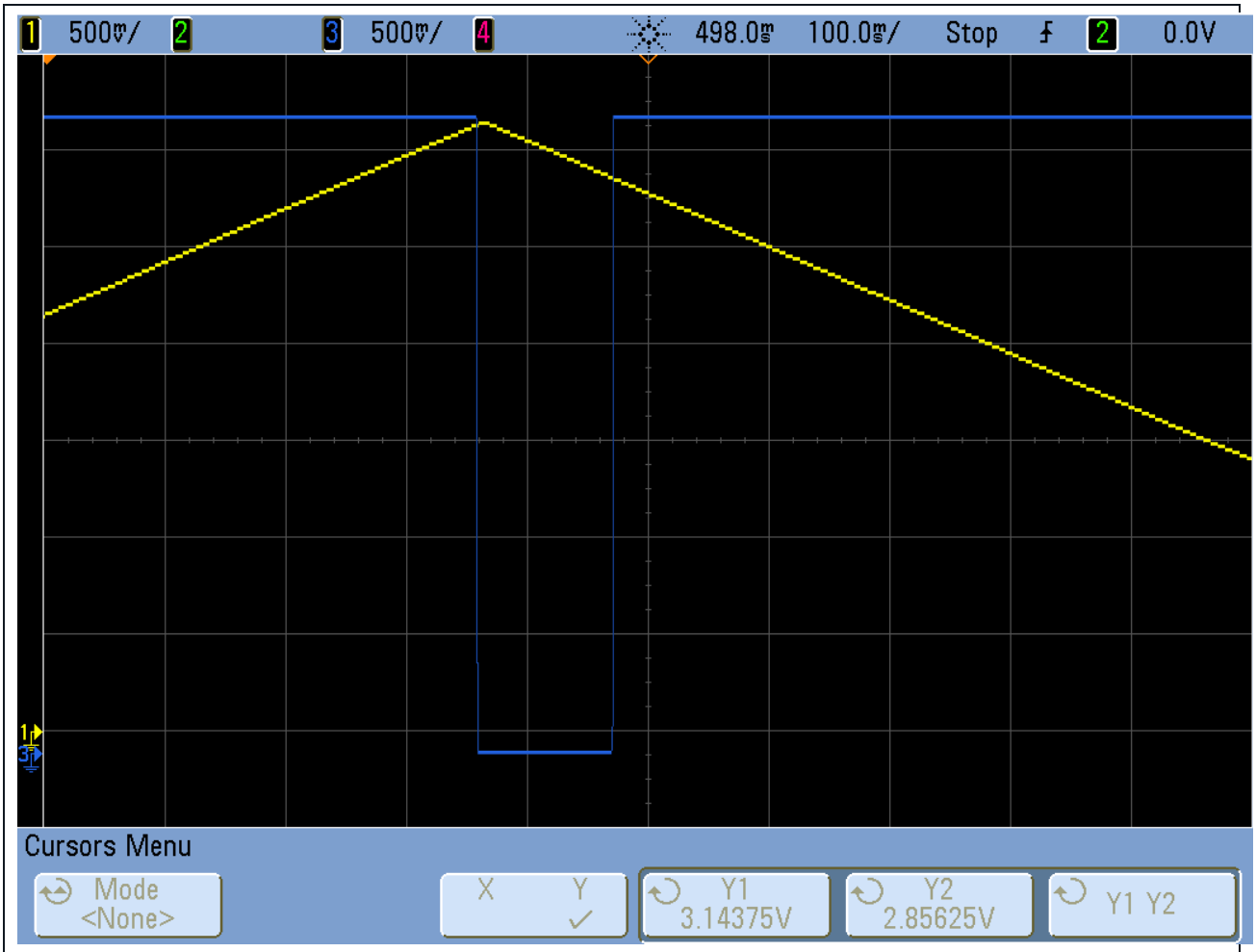
The input of the hysteresis comparator originates from an amplifier described in the analog section. The transfer ratio of the amplifier is 7.04 mV/V. Considering this, the V_L and V_H values referenced to the following DCP values:

$$V_{Href} = \frac{V_H}{7{,}04\ {}^{mV}/_{V}} = 400\ V$$

$$V_{Lref} = \frac{V_L}{7{,}04\ {}^{mV}/_{V}} = 440\ V$$

This signal is then latched into IC17, which can be reset by the microcontroller GPIO7 pin. The reset signal can be observed at RST (TP18), the output of the latch with negative logic at VDC-FAULT (TP30).



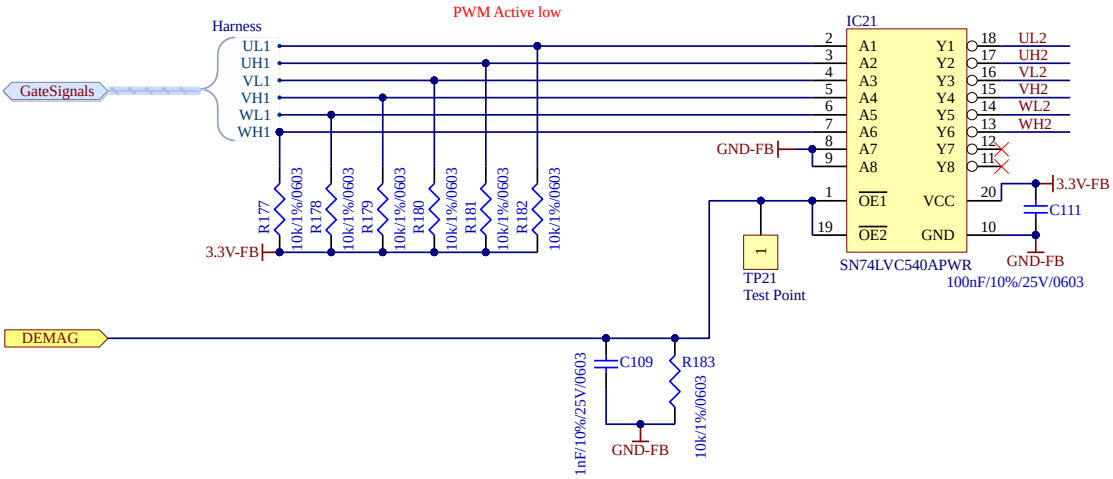


Voltage hysteresis of the over voltage comparator

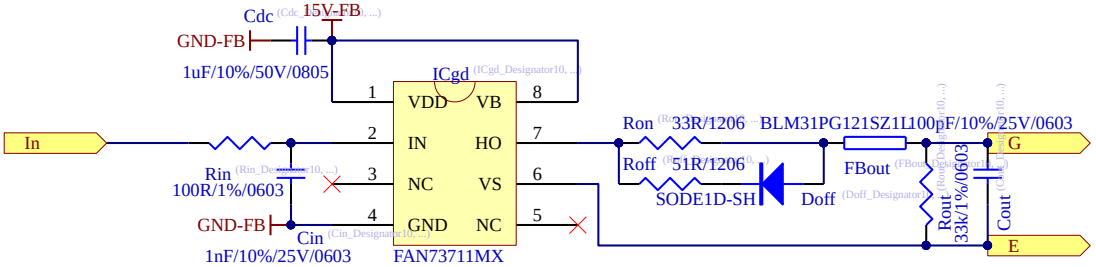
The simulated DC link voltage (yellow) trips the comparator output (blue) and resets it at a different voltage level.

5.5 Three-Phase inverter

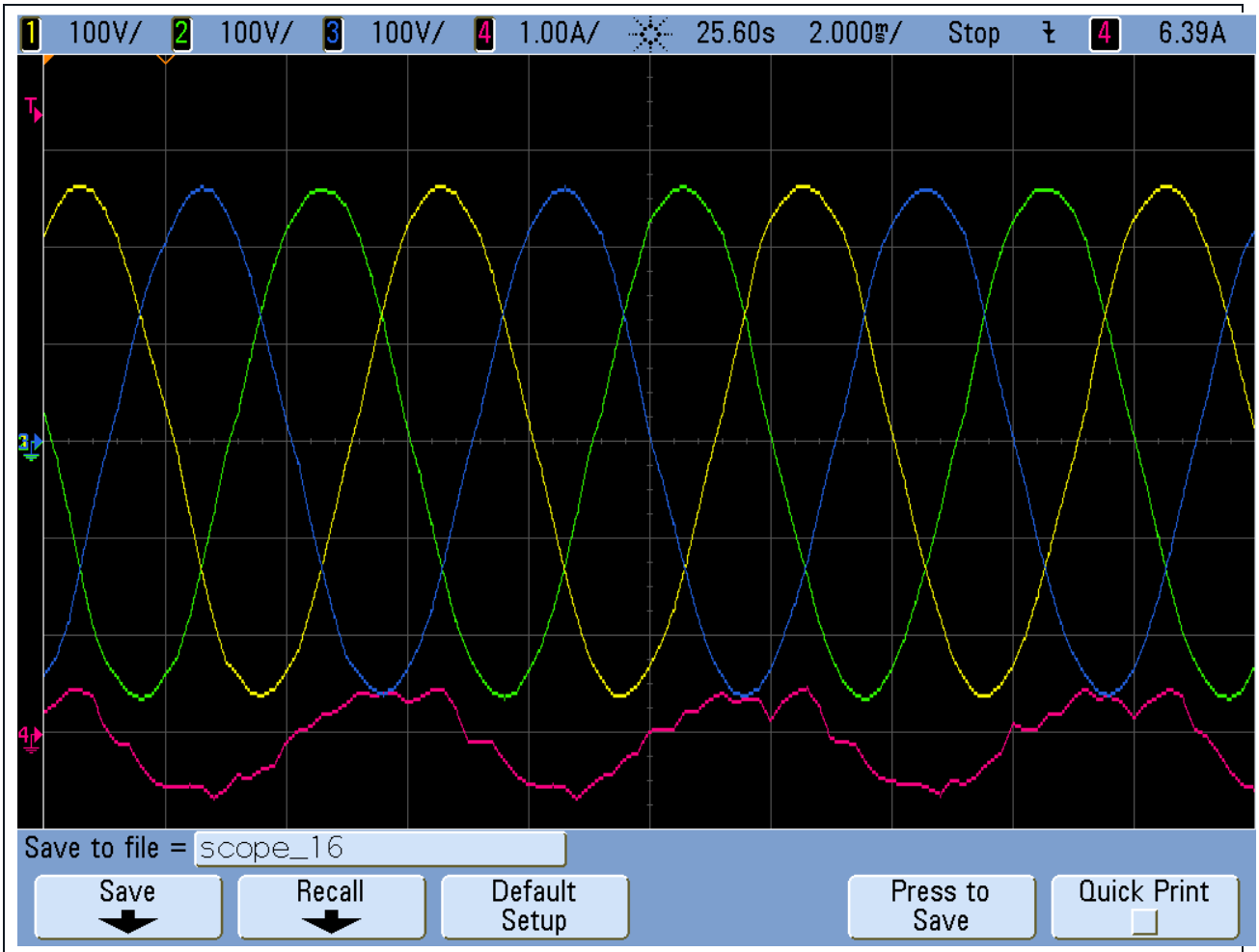
The three-phase inverter contains the FAN73711MX gate drivers for each IGBT. The SN74LVC540APWR buffer is used to disable the inverter in case of DEMAG protection. The FAN73711MX is a high current high side gate driver. It is configured as a high side driver for the inverter's upper IGBTs and as a low side for the lower IGBTs. The driver has built-in level shifter, noise filtering and under voltage lockout. All three phases have low side emitter shunts in order to measure the current for the MCU (further description in the MCU section).



The DEMAG protection is presented in the previous chapter and its output can be observed at DEMAG test point (TP21). The gate signals are connected to the corresponding gate driver ICs.

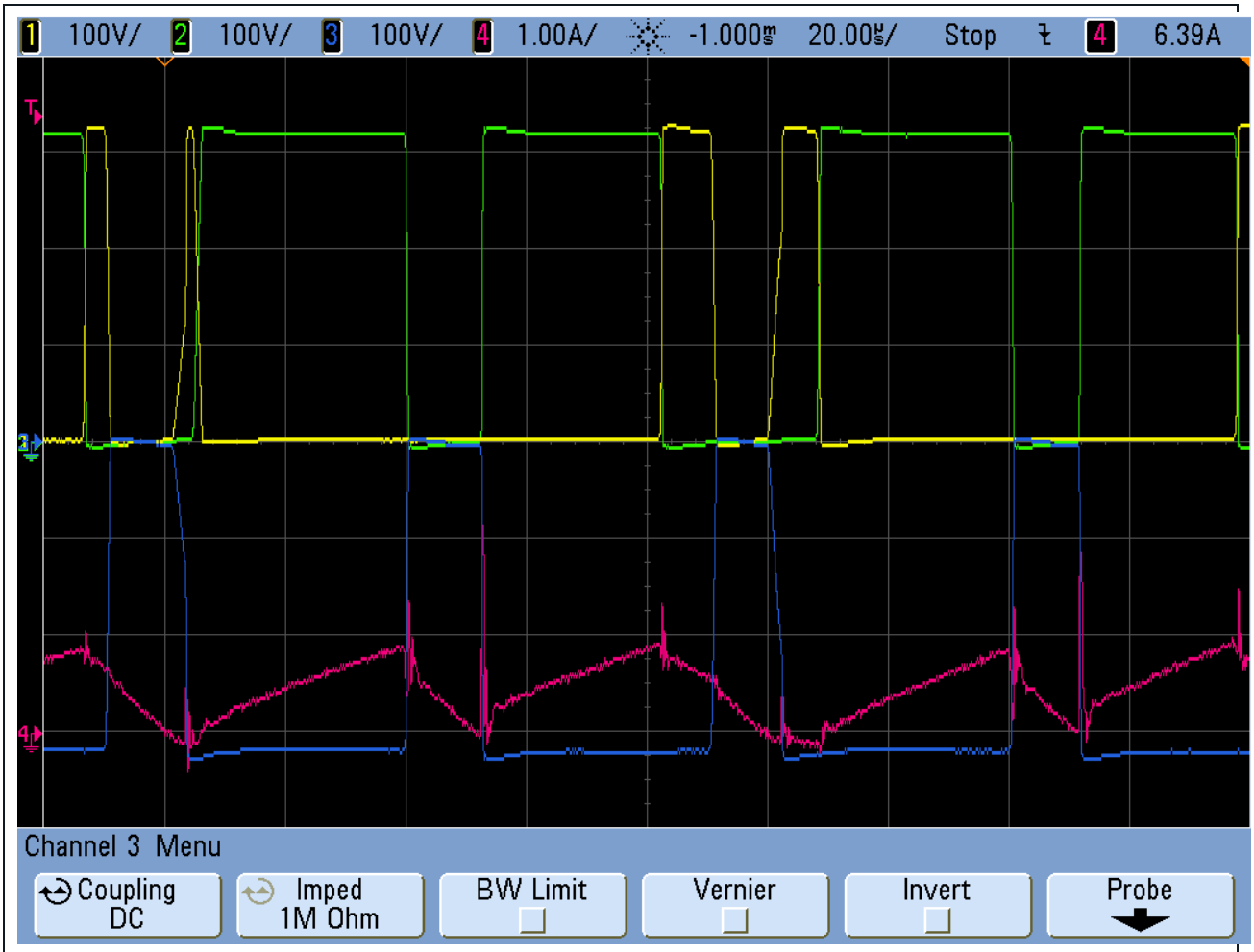


Filtering on the input is done with an RC filter. Each Driver IC has its own decoupling capacitor. The diodes on the output of the gate driver ICs set the turn-on and turn-off gate resistance to different values. The output current from the IC (turn-on event) is blocked by the diode therefore only the R_{on} resistor is in the gate loop. The R_{gon} is 33 Ω. During turn-off the on and off resistors are connected in parallel and the resulting resistance of 20 Ω turns off the transistor. On the output a ferrite bead is used. In combination with the capacitor it creates a LC filter.



Inverter output waveforms

With SPWM modulation a sine output voltage average can be achieved on the output of the inverter. This measurement was done with differential probes on the three-line voltage which is provided to a permanent magnet motor (LAFERT HPS 71 3600 72) with no load. The phase current (purple) is measured at the u phase. The voltage measurements are the following order: V_{VW} (yellow), V_{UV} (green), V_{WU} (blue). 3rd harmonic modulation was used.



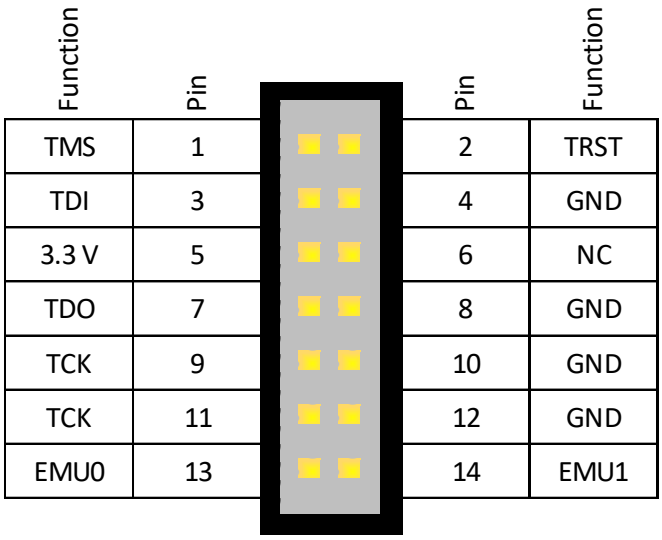
switching waves

The switching events of the previous setup can be seen above.

5.6 Interface to the MCU

The TMS320F28027FPTT microcontroller is driven by an external ceramic resonator (CT1) CSTCE10M0G15C99-R0. It provides a stable 10 MHz clock signal for the MCU.

The JTAG is disabled for normal operation on TRST by pin a pull-down resistor (R301). The pin can be pulled high externally on pin2 of CN5 connector. All other pins of the JTAG interface can be accessed on the connector including two emulation references. The connector is compliant to TI's design recommendation and IEEE 1149.1 standard.



Function	Pin		Pin	Function
TMS	1		2	TRST
TDI	3		4	GND
3.3 V	5		6	NC
TDO	7		8	GND
TCK	9		10	GND
TCK	11		12	GND
EMU0	13		14	EMU1

Figure 2: Pin mapping of CN5 connector

The reset pin (XRS) is pulled to 3.3 V with an RC circuit (C113 and R199).

The internal voltage regulator is enabled (VREGENZ). The analog channels measure the AC input voltage, PFC current for each leg, DC-link voltage, output phase voltage, current and NTC voltage.

Channel	Symbol	Description
A0	3,3V	3,3V rail
A1	Vout-V	V phase output voltage
A2	Vout-U	U phase output voltage
A3	Vout-W	W phase output voltage
A4	IPFC2	PFC leg2 current
A6	IPFC1	PFC leg1 current
A7	IPFC3	PFC leg3 current
B1	IW	W phase current
B2	IV	V phase current
B3	IU	U phase current
B4	VDC	DC-link voltage
B6	NTC	PIM thermistor voltage
B7	VAC	AC input voltage

All gate drivers are connected to an enhanced PWM unit.

EPWM Ch	Gate
EPWM1A	UH1
EPWM1B	UL1
EPWM2A	VH1

EPWM2B	VL1
EPWM3A	WH1
EPWM3B	WL1

The parameters (32K x 8bit) can be stored in an external I2C EEPROM BR24T256FVT-W (IC24). The serial communication and the EEPROM can be reached thru the built-in hardware serial interfaces.

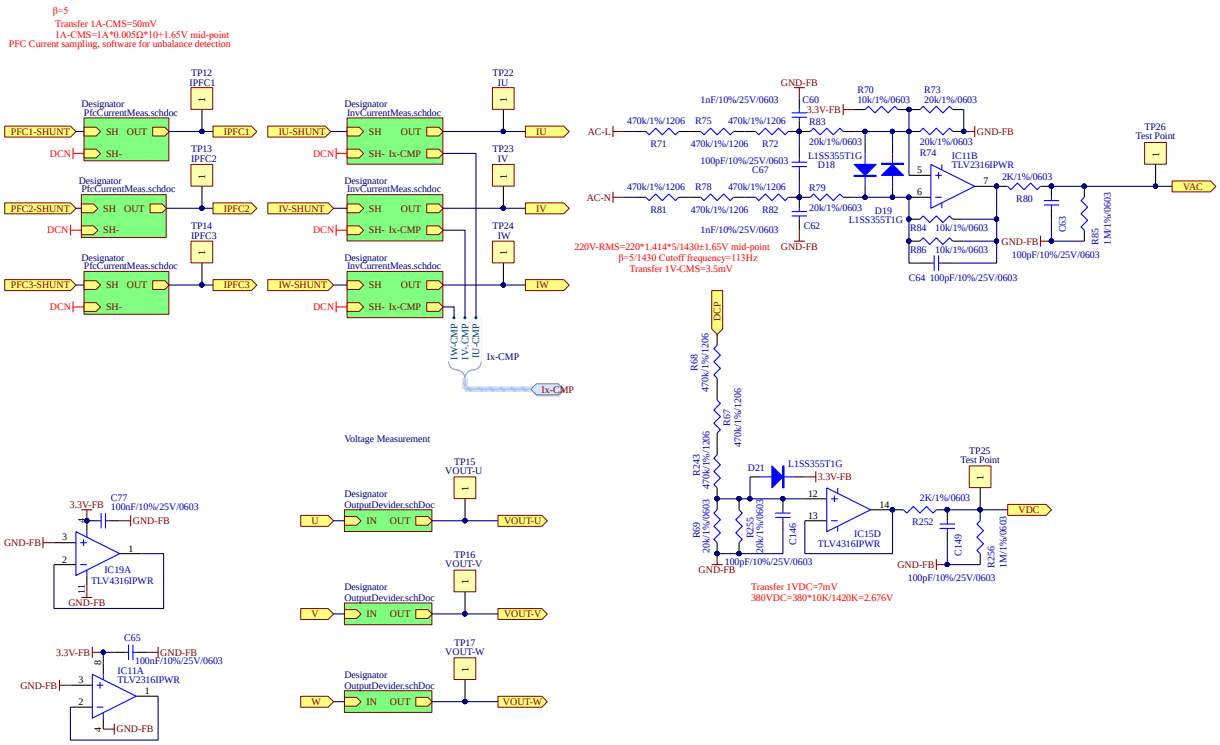
Interface	Device
I2C	EEPROM
SCI	RS485 COMMUNICATION

The general inputs and outputs are connected to the remaining pins of the controller. Input pins can be assigned to trip zones to react to their state changes in real time.

GPIO	Function	I/O	TripZone
GPIO6	DSB-PFC	IN	
GPIO7	RST	OUT	
GPIO12	VDC-FAULT	IN	TZ1
GPIO16	LED	OUT	
GPIO17	RDE	OUT	
GPIO28	INV-FAULT	IN	TZ2
GPIO29	PTC-CON	OUT	
GPIO34	PFC-EN	OUT	

5.6.1 Analog measurement

For controlling the inverter analog signals have to be measured by the MCU's ADC. The analog channels, to which the signals are connected, were described in the previous chapter. This chapter gives a deep explanation on the different channel's transfer functions.



The input AC voltage, PFC leg current, DC-link voltage, output phase voltage and inverter phase DC- current are measured.

The input AC voltage is measured by a differential amplifier circuit. The non-inverting input is referenced to mid voltage of the 3.3 V rail (R70, R73 and R74). This creates an offset to the output in order to be able to measure negative voltage on the input. Given that

$$R_{70} \times (R_{73} \times R_{74}) = R_{84} \times R_{86} \; and \; R_{71} + R_{75} + R_{72} + R_{83} = R_{81} + R_{78} + R_{82} + R_{79}$$

the output can be calculated with the following calculation.

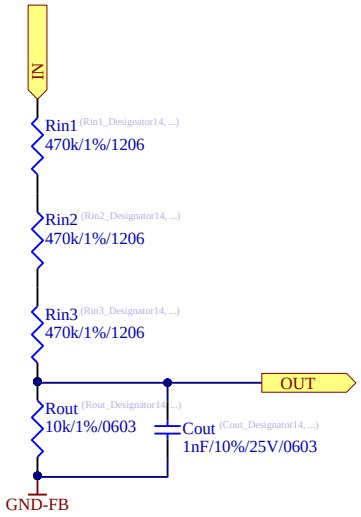
$$V_{VAC} = (V_{AC-L} - V_{AC-N}) \frac{R_{84} \times R_{86}}{R_{81} + R_{78} + R_{82} + R_{79}} + V_{3.3V} \frac{(R_{73} \times R_{74})}{(R_{73} \times R_{74}) + R_{70}}$$

The transfer function of the amplifier:

$$V_{out} = V_{in} \frac{5k}{1430k} + 3.3 \frac{10k}{10k + 20k \times 20k} = \frac{V_{in}}{286} + 1.65V$$

The PFC current to voltage ratio is 3.5 mV/V offset by 1.65 V. The input differential voltage is clamped with a pair of antiparallel diodes. To reject high frequency noise a filter is utilized. The input divider's resistors in combination with C60 and C62 form a low pass filter with a cutoff frequency of 133 Hz.

Each output phase voltage is measured directly via a voltage divider.



The output voltage to ADC ratio can be calculated with the following equation and relative to FB-GND:

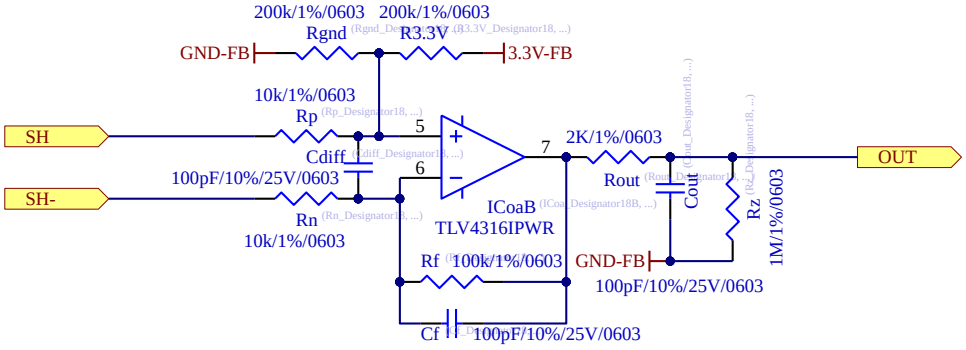
$$V_{out} = V_{in}\frac{R_{out}}{\sum R_{in} + R_{out}} = V_{in}\frac{10k}{3 \cdot 470k + 10k} = V_{in}\frac{10}{1420} = V_{in} \cdot 7m$$

The transfer is 1 V/7 mV. Consider 380 V DC link voltage

$$V_{out} = 380\,V \cdot \frac{10}{1420} = 2.676\,V$$

The output phase voltage feedback $V_{out\text{-}U}$, $V_{out\text{-}V}$, $V_{out\text{-}W}$ can be measured on (TP15, TP16, and TP17). The DC-link voltage is measured similarly and buffered with a voltage follower amplifier and clamped to the 3.3 V rail. It can be measured on TP25.

Inverter and PFC shunt current measurement is done by a differential amplifier.



The non-inverting input is referenced to mid voltage of the 3.3 V rail (R_{gnd},$R_{3.3V}$). It offsets the output in order to measure negative current on the shunt with a single-ended input. Given that

$$R_{gnd} \times R_{3.3V} = R_f \; and \; R_n = R_p$$

the output can be calculated with the following calculation:

$$V_{out} = (V_{SH} - V_{SH-})\frac{R_f}{R_n} + V_{3.3V}\frac{R_{gnd}}{R_{gnd} + R_{3.3V}}$$

The voltage drop on the shunt is:

$$V_{shunt} = R_{shunt} \cdot I = 0.005\Omega \cdot I$$

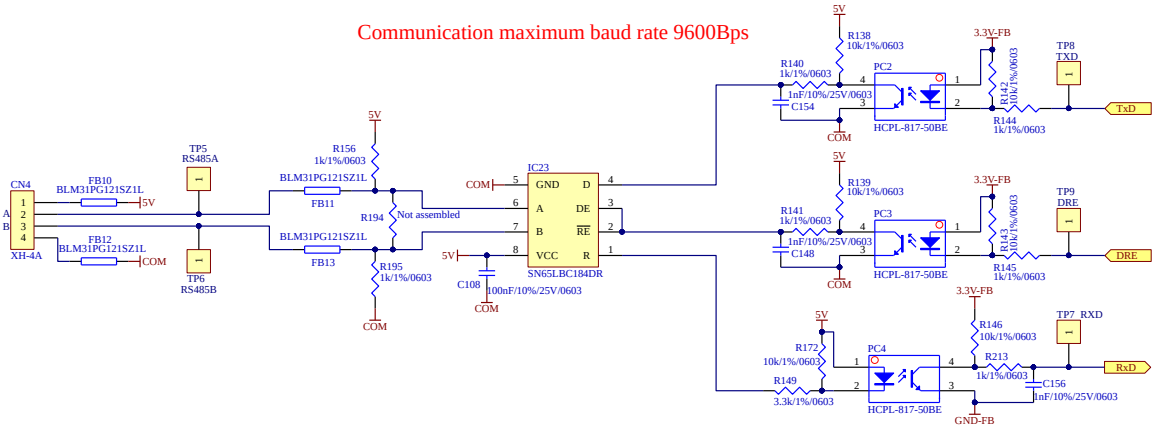
Finally, the transfer function of the amplifier (PFC):

$$V_{out} = (0.005 \cdot I)\frac{10k}{100k} + 3.3\frac{200k}{200k + 200k} = 0.05I + 1.65V$$

The PFC current to voltage ratio is 50 mV/A offset by 1.65 V The Inverter current to voltage ratio is 25 mV/A offset by 1.65 V.

5.6.2 Communication

Fully isolated serial communication is used to control the inverter externally (e.g. HMI / service). This interface is realized with a RS485 line driver (IC23) and opto couplers for isolation. The secondary side of the communications section has its own isolated power supply (see in aux power supply chapter). The receiver, transmitter and direction signals are galvanically isolated from the MCU which is referenced to the high voltage ground.



The opto isolators PC2, PC3 and PC4 (HCPL-817-50BE) offer 5000 V isolation. The line driver is a differential transceiver SN65LBC184DR, which is compliant with the RS-485 specification. It also has built-in voltage suppression, thermal protection and power-rail glitch protection. All lines has ferrite beads for noise cancelling. The output of the RS-485 communication can be connected via CN4, which has also the 5 V power and GND reference. The output signal can be measured at TP5 (A) and TP6 (B) and must be referenced to the isolated ground at TP3 (COM).

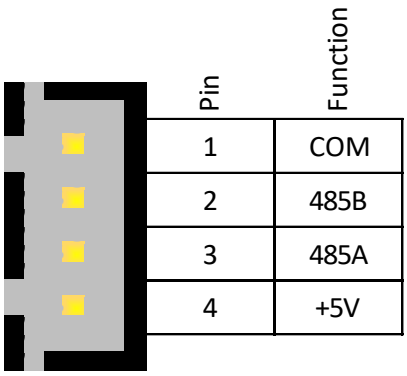


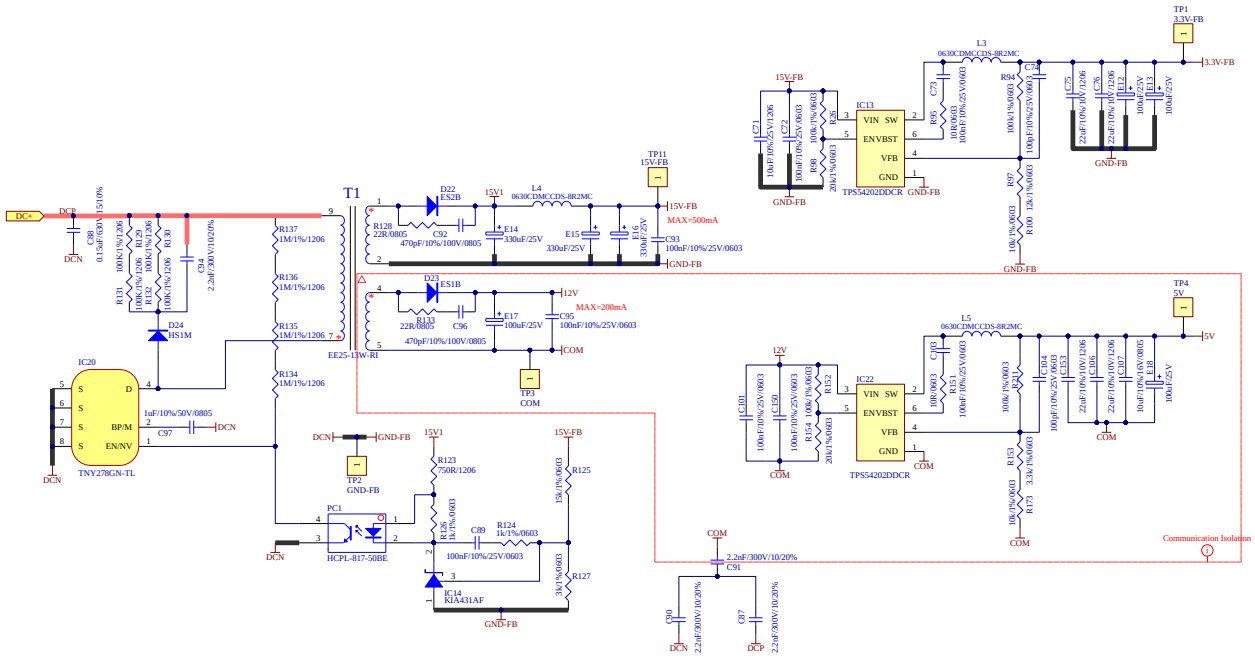
Figure 3: Pin mapping of CN4 connector

The connection to the MCU is an ordinary duplex serial line communications by a direction input (DRE). In case of DRE is on a high level the data direction is set to output and data can be transmitted on TxD line. When the DRE is low, the differential transceiver is set to receive data to RxD line on the MCU. These signals can be observed on TP7 (RxD), TP8 (TxD) and TP9 (RDE) and must referenced to the MCU's ground at TP2 (GND-FB).

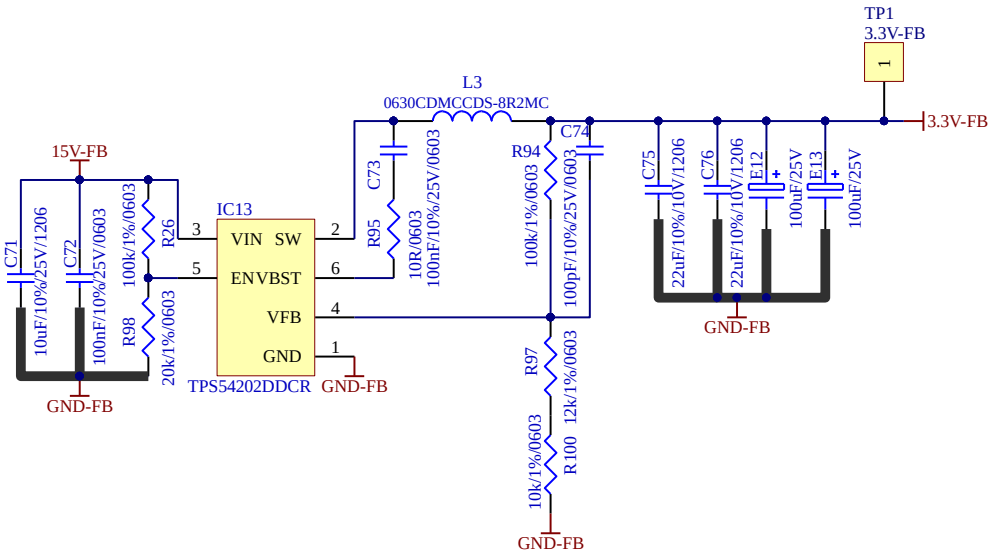
These points are at 3.3 V voltage level.

5.7 Auxiliary Power supply

For the control circuitry several voltage rails have to be supplied. The DC link voltage have to be lowered, and regulated. The rail for the communication have to be isolated from the high voltage.



The TNY278 flyback controller (IC20) regulates and switches the current on the T1 transformer. The two windings on the secondary side of the transformer create two separate voltage rails: One for the control circuitry and one for the isolated side of the communication. The feedback of the converter is referenced to the 15 V rail (15V-FB) and feeds back on PC1 opto-coupler. The 15 V rail can be measured on TP11. A 3.3 V rail is created from the 15 V supply for the control circuitry. The TPS54202DDCR buck regulator is a 500 kHz synchronous buck converter. It needs few complementary parts. The feedback resistors R94, R97 and R100 set the desired 3.3 V output voltage for the converter.



$$V_{out} = \frac{V_{FB} \cdot (R94 + R97 + R100)}{R97 + R100}$$

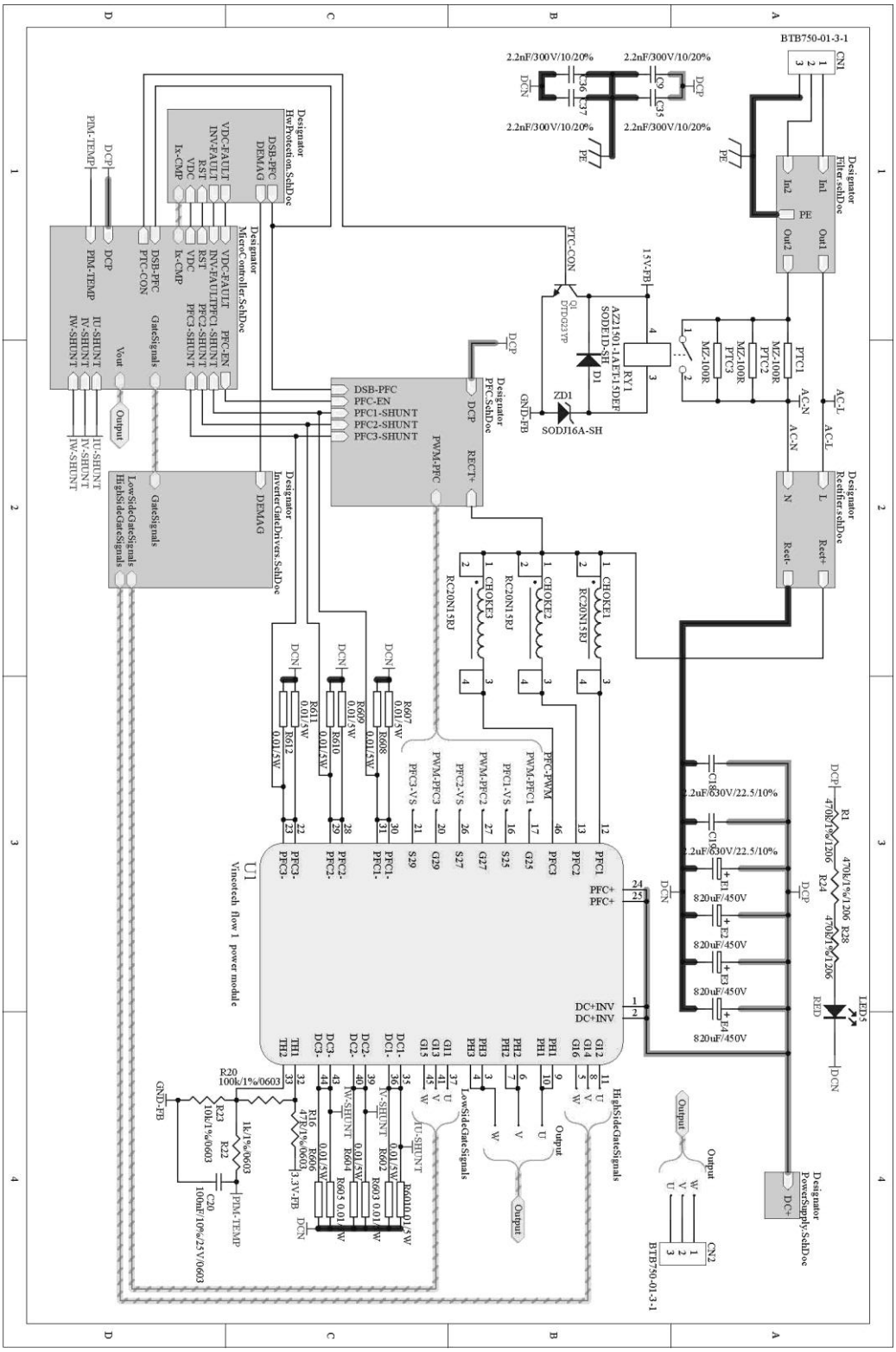
$$V_{out} = \frac{0{,}596 \cdot (100k + 12k + 10k)}{12k + 10k} = 3{,}3\ V$$

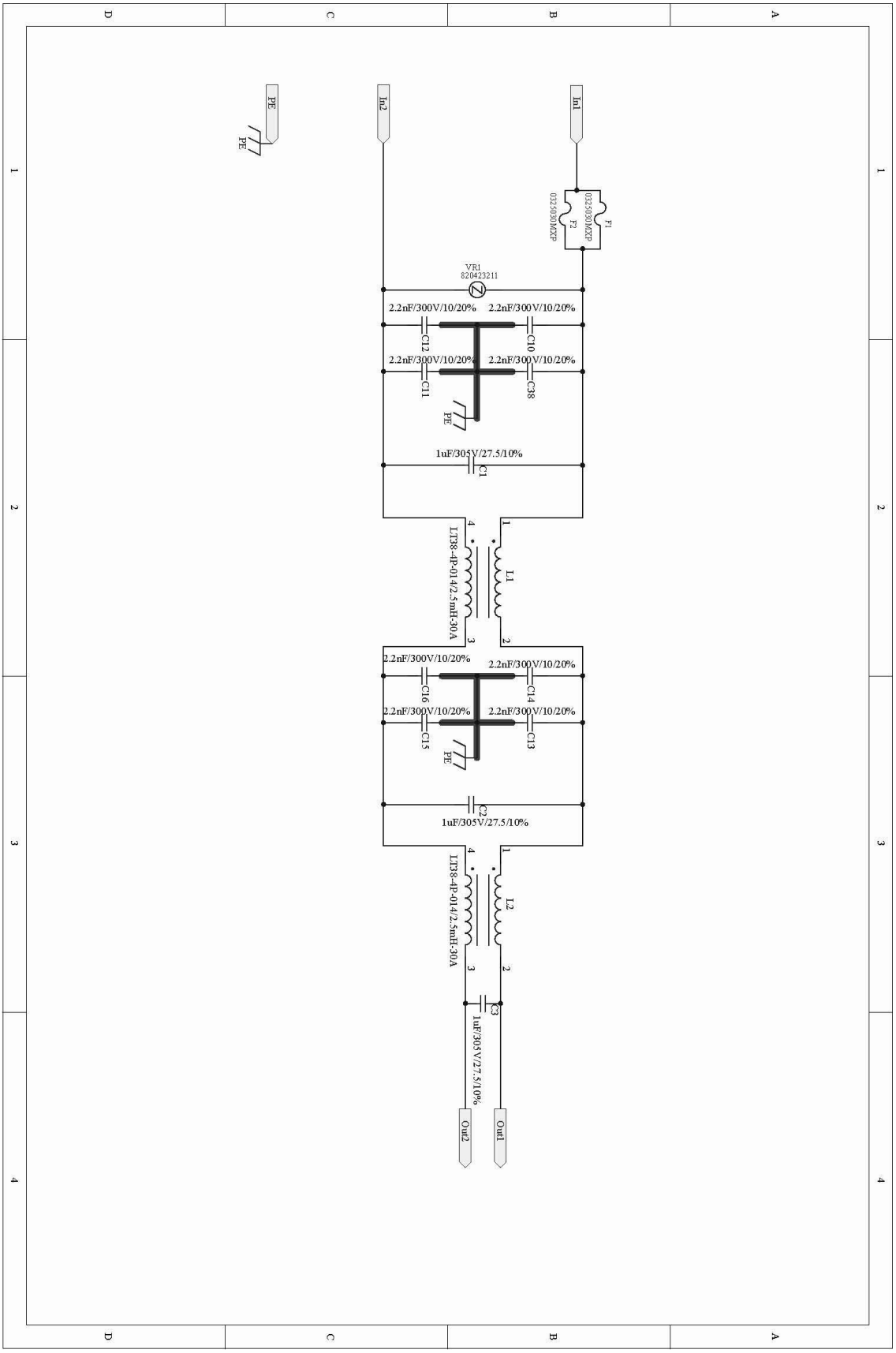
For the inductor (L3) a 8.2 µH inductor is used. Its peak current value is well below the saturation current.

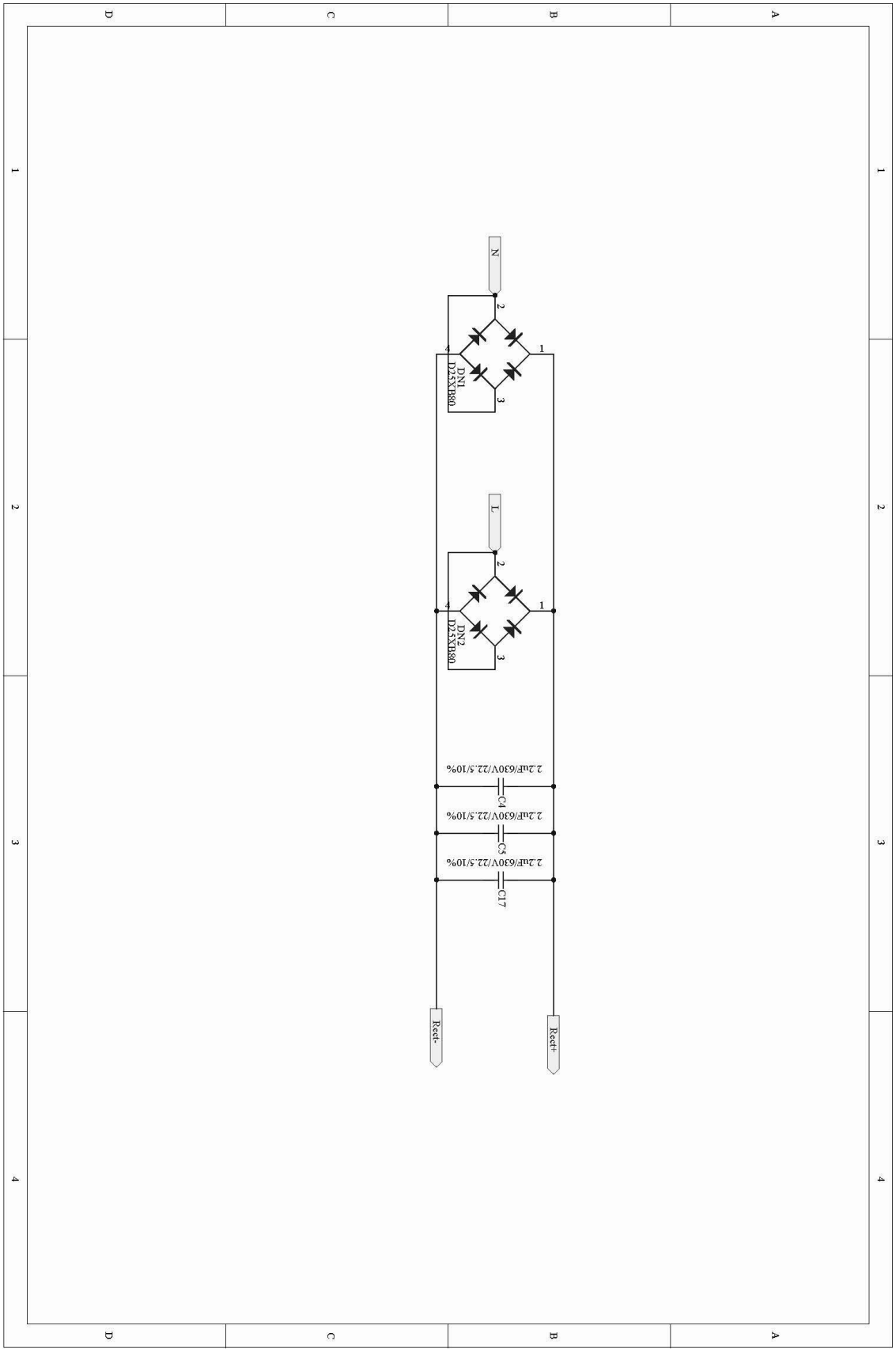
$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{1{,}6 \cdot V_{IN(MAX)} \cdot L_{OUT} \cdot f_{sw}}$$

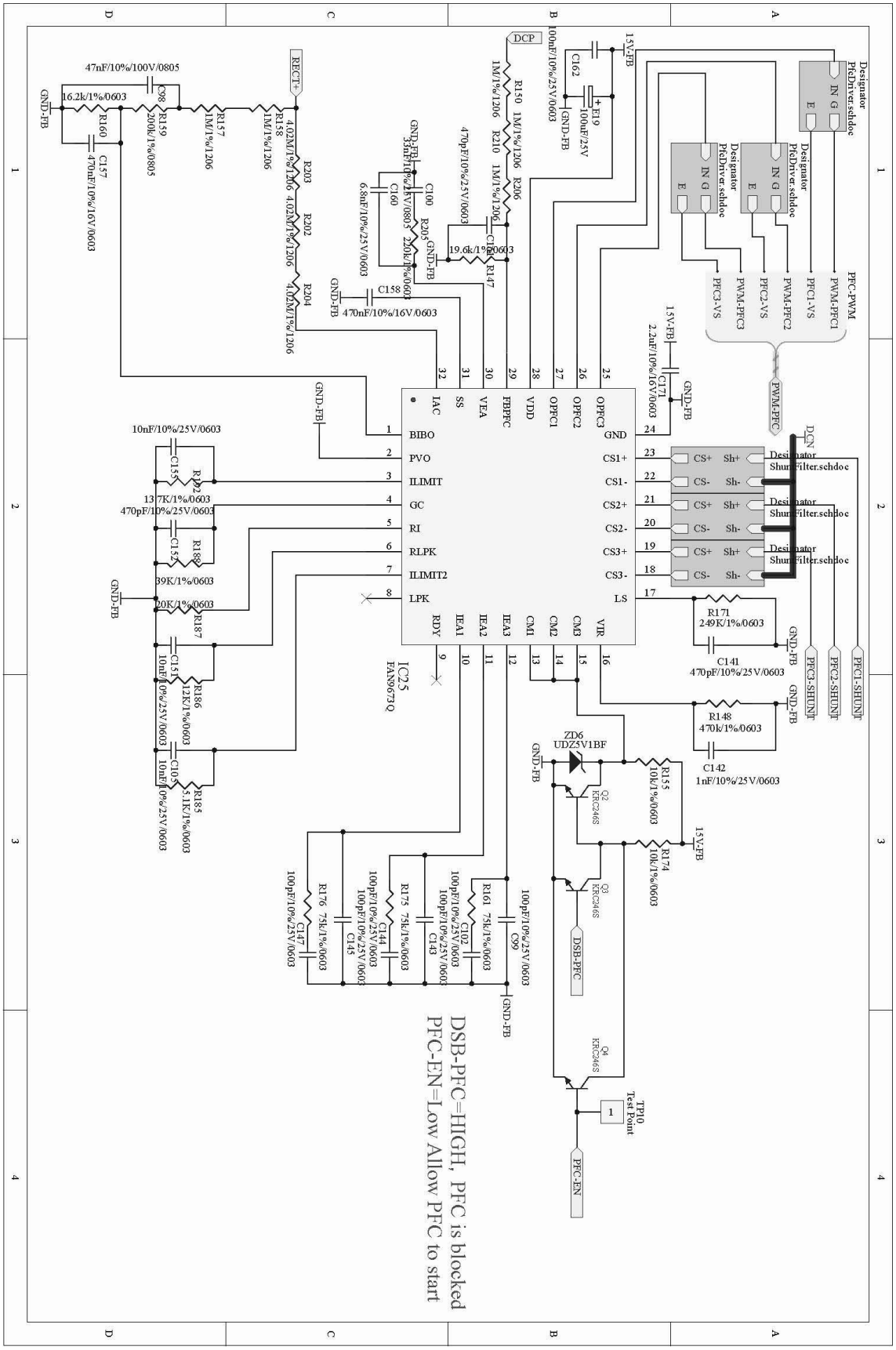
$$I_{L(PK)} = 0{,}5 + \frac{3{,}3 \cdot (15 - 3{,}3)}{1{,}6 \cdot 15 \cdot 8{,}2\mu \cdot 500k} = 892mA$$

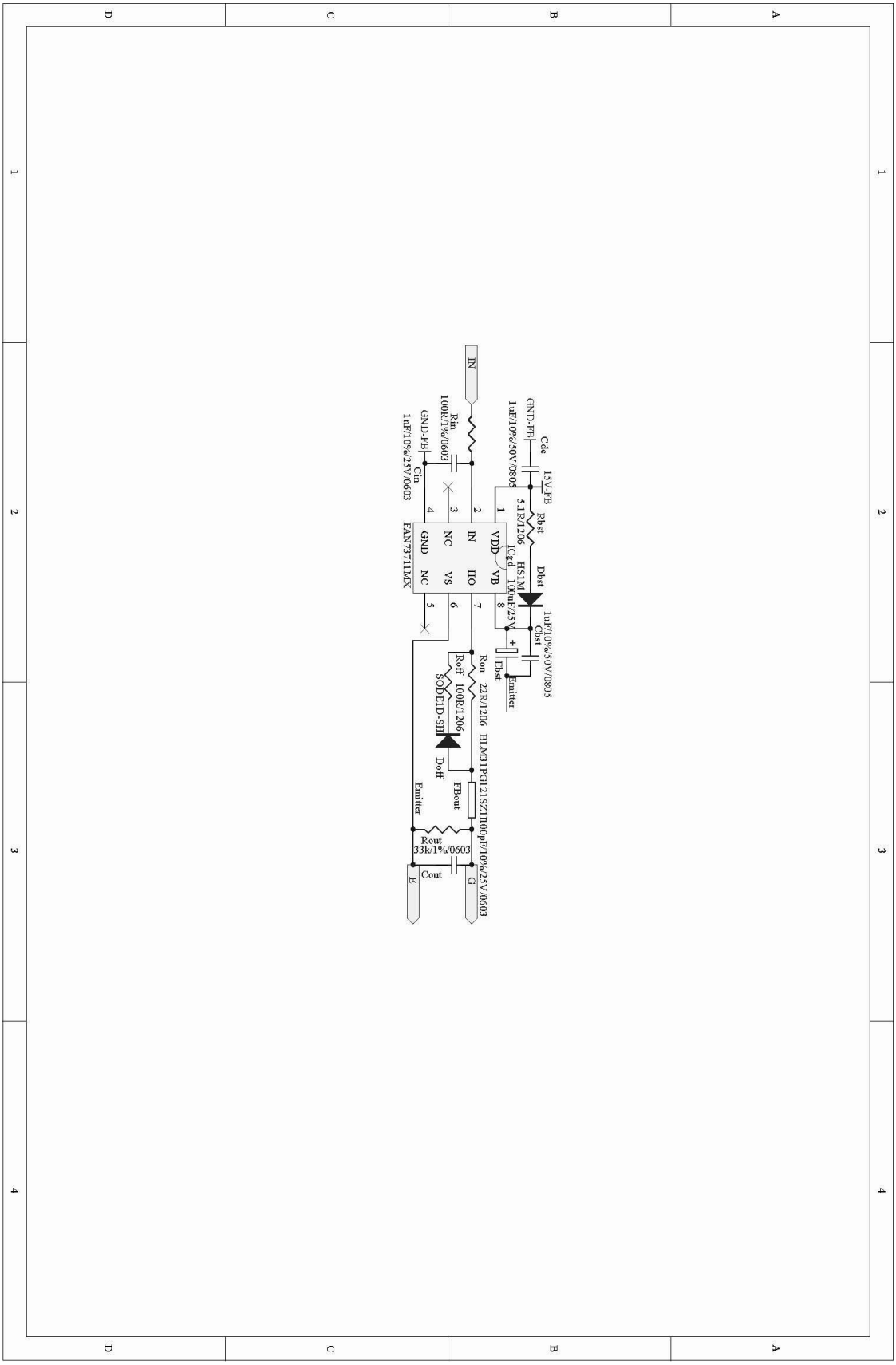
6 Schematic

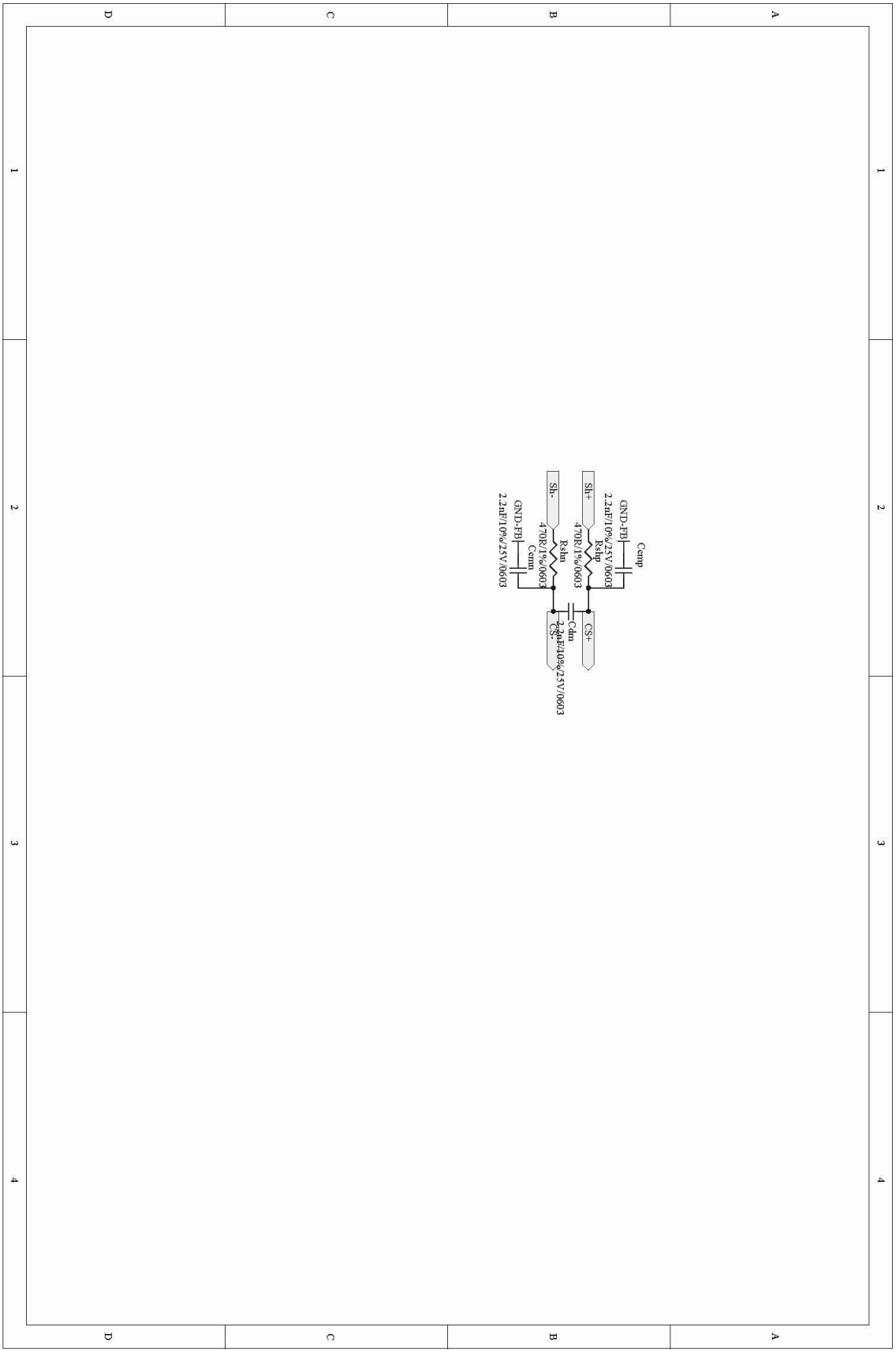

BTB750-01-3-1
CN1
2.2nF/300V/10/20%
C36
C37
C9
C35
DCN
DCP
PE
Designator Filter.schDoc
In1
In2
PE
Out1
Out2
MZ-100R
PTC1
PTC2
PTC3
AC-L
AC-N
Designator Rectifier.schDoc
L
N
Rect+
Rect-
15V-FB
PTC-CON
Q1 DTD123YP
AZ21901-1AE7-1SDEF SOD5ED-SH
RY1
D1
ZD1
SODJ16A-SH
GND-FB
Designator PFC.SchDoc
DSB-PFC
PFC-EN
PFC1-SHUNT
PFC2-SHUNT
PFC3-SHUNT
DCP
RECT+
PWM-PFC
CHOKE1
CHOKE2
CHOKE3
RC20N15RJ
Designator HwProtection.SchDoc
DSB-PFC
DEMAG
VDC-FAULT
INV-FAULT
RST
VDC
Ix-CMP
Designator MicroController.SchDoc
PFC-EN
PFC1-SHUNT
PFC2-SHUNT
PFC3-SHUNT
GateSignals
Vout
IU-SHUNT
IV-SHUNT
IW-SHUNT
PIM-TEMP
Output
Designator InverterGateDriven.SchDoc
LowSideGateSignals
HighSideGateSignals
R607
R608
R609
R610
R611
R612
0.01/5W
PFC-PWM
PWM-PFC1
PWM-PFC2
PWM-PFC3
PFC1-VS
PFC2-VS
PFC3-VS
U1
Vincotech flow 1 power module
PFC+
DC+INV
PFC1
PFC2
PFC3
PFC2-
PFC3-
PFC1-
S25
S27
S29
G25
G27
G29
PB1
PB2
PB3
GI1
GI3
GI5
GI2
GI4
GI6
DC1-
DC2-
DC3-
TH1
TH2
U-SHUNT
V-SHUNT
W-SHUNT
R602
R603
R604
R605
R606
R20
100k/1%/0603
R23
10k/1%/0603
R22
1K/1%/0603
R16
47R/1%/0603
C20
100nF/10%/25V/0603
3.3V-FB
C18
C19
2.2uF/630V/22.5/10%
E1
E2
E3
E4
820uF/450V
R1
R24
R28
470k/1%/1206
LED5
RED
Designator PowerSupply.SchDoc
DC+
CN2
BTB750-01-3-1

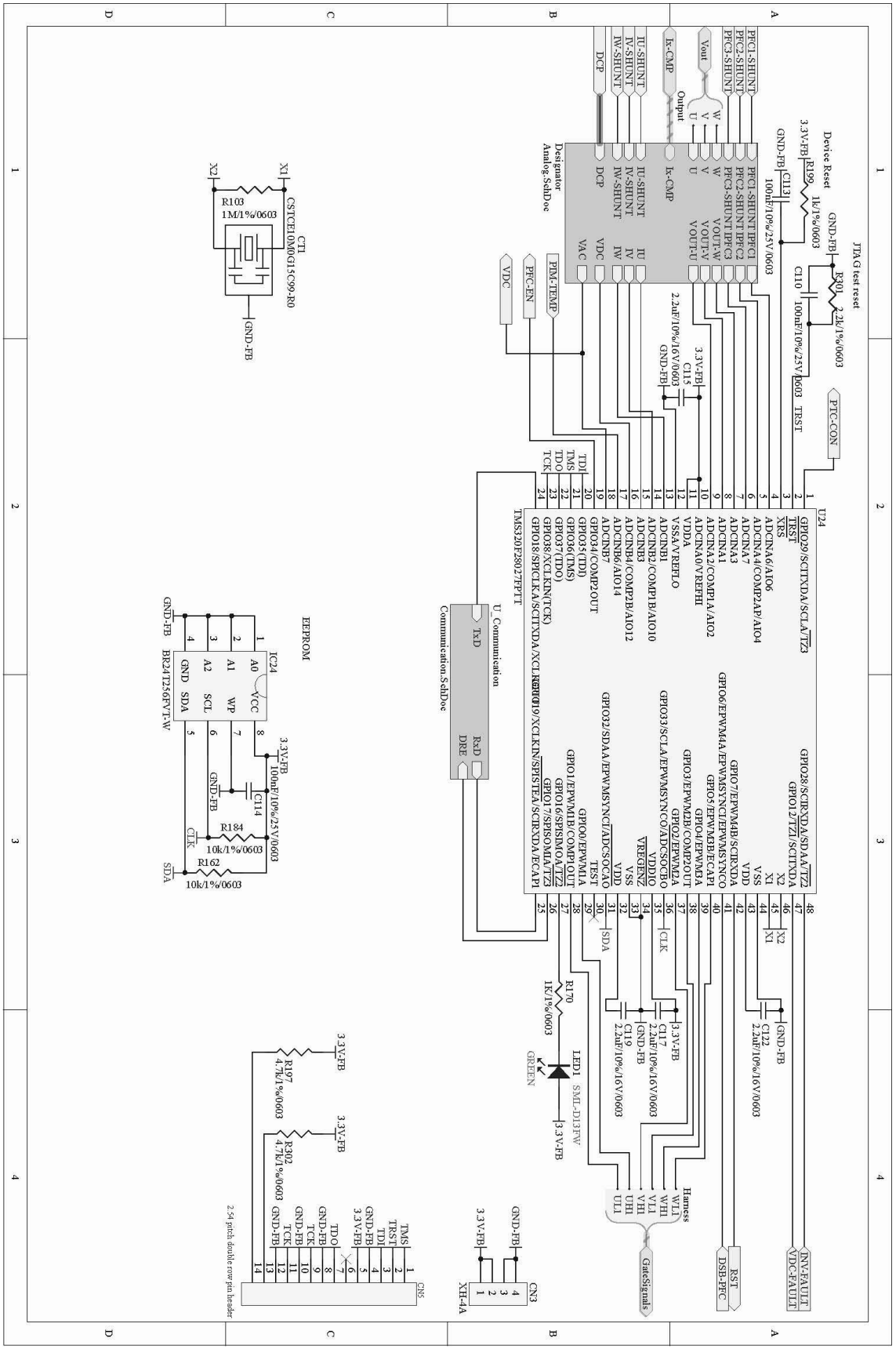

PE
PE
In2
In1
0325030MXP
F1
F2
0325030MXP
VR1
820423211
2.2nF/300V/10/20%
2.2nF/300V/10/20%
C12
C10
2.2nF/300V/10/20%
2.2nF/300V/10/20%
C11
C38
PE
1uF/305V/27.5/10%
C1
LT38-4P-014/2.5mH-30A
L1
2.2nF/300V/10/20%
2.2nF/300V/10/20%
C16
C14
2.2nF/300V/10/20%
2.2nF/300V/10/20%
C15
C13
PE
C2
1uF/305V/27.5/10%
LT38-4P-014/2.5mH-30A
L2
C3
1uF/305V/27.5/10%
Out2
Out1

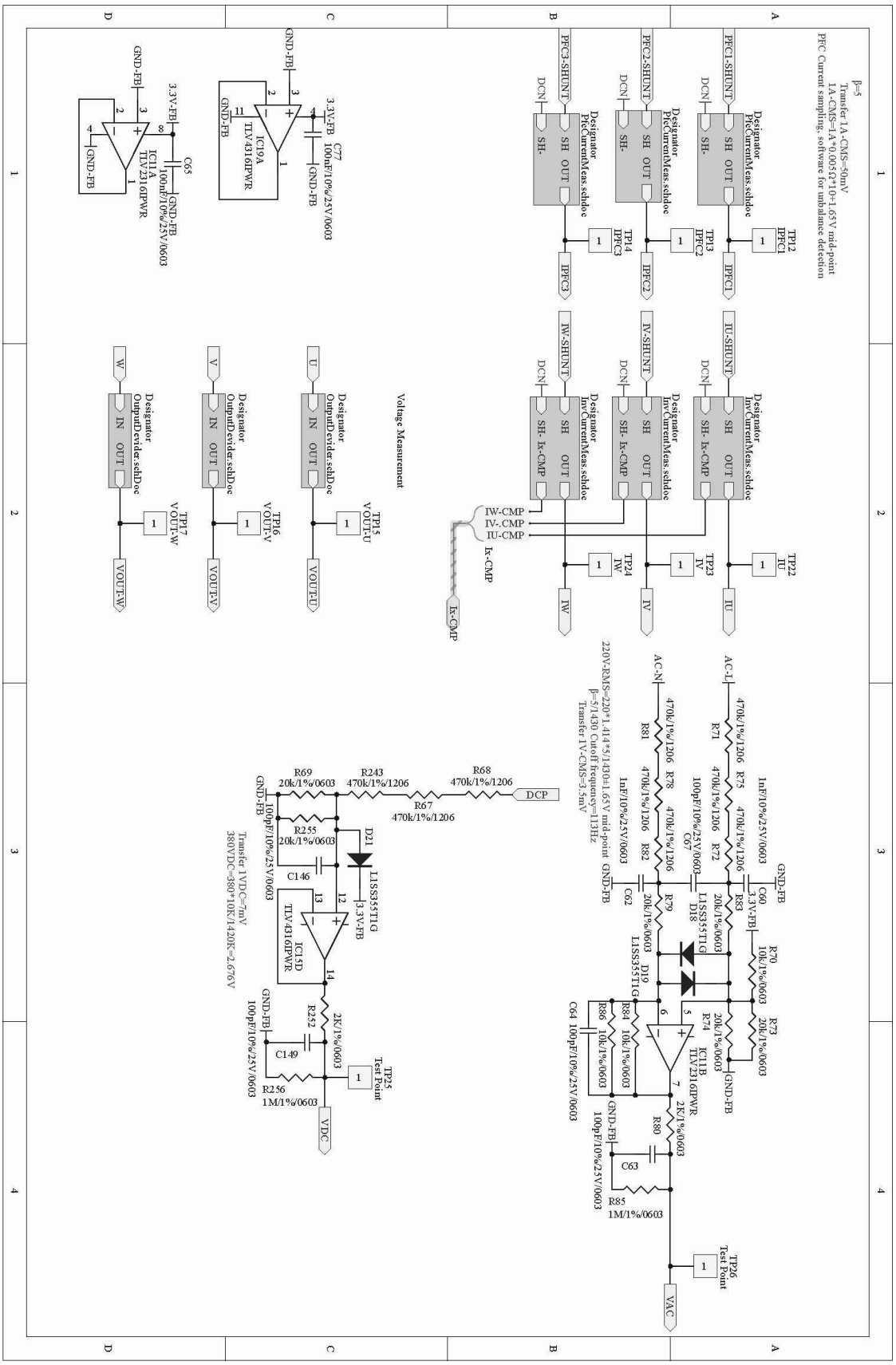

N
L
DN1
D25XB80
DN2
D25XB80
2.2uF/630V/22.5/10%
C4
2.2uF/630V/22.5/10%
C5
2.2uF/630V/22.5/10%
C17
Rect-
Rect+

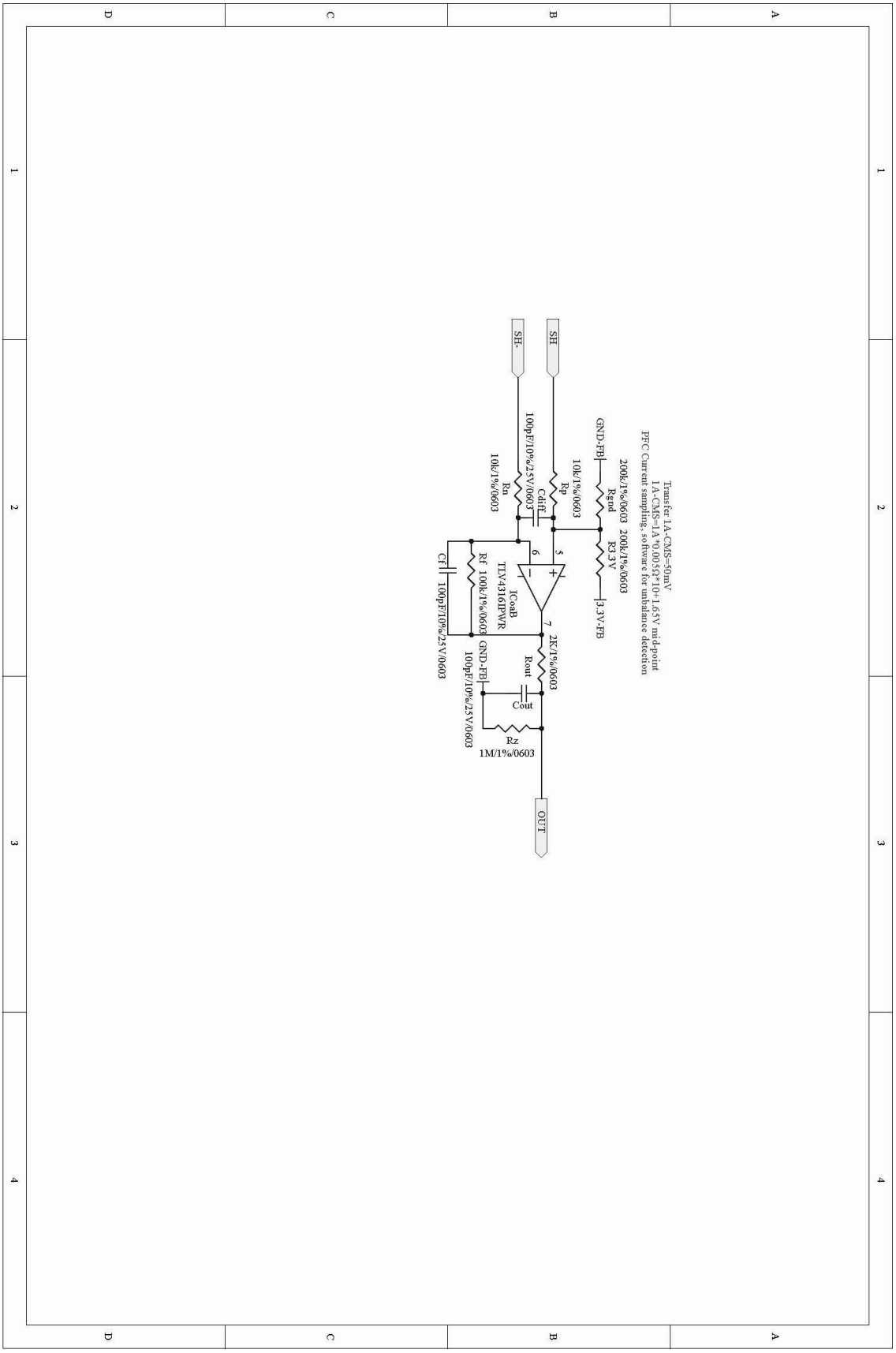

DSB-PFC=HIGH, PFC is blocked
PFC-EN=Low Allow PFC to start

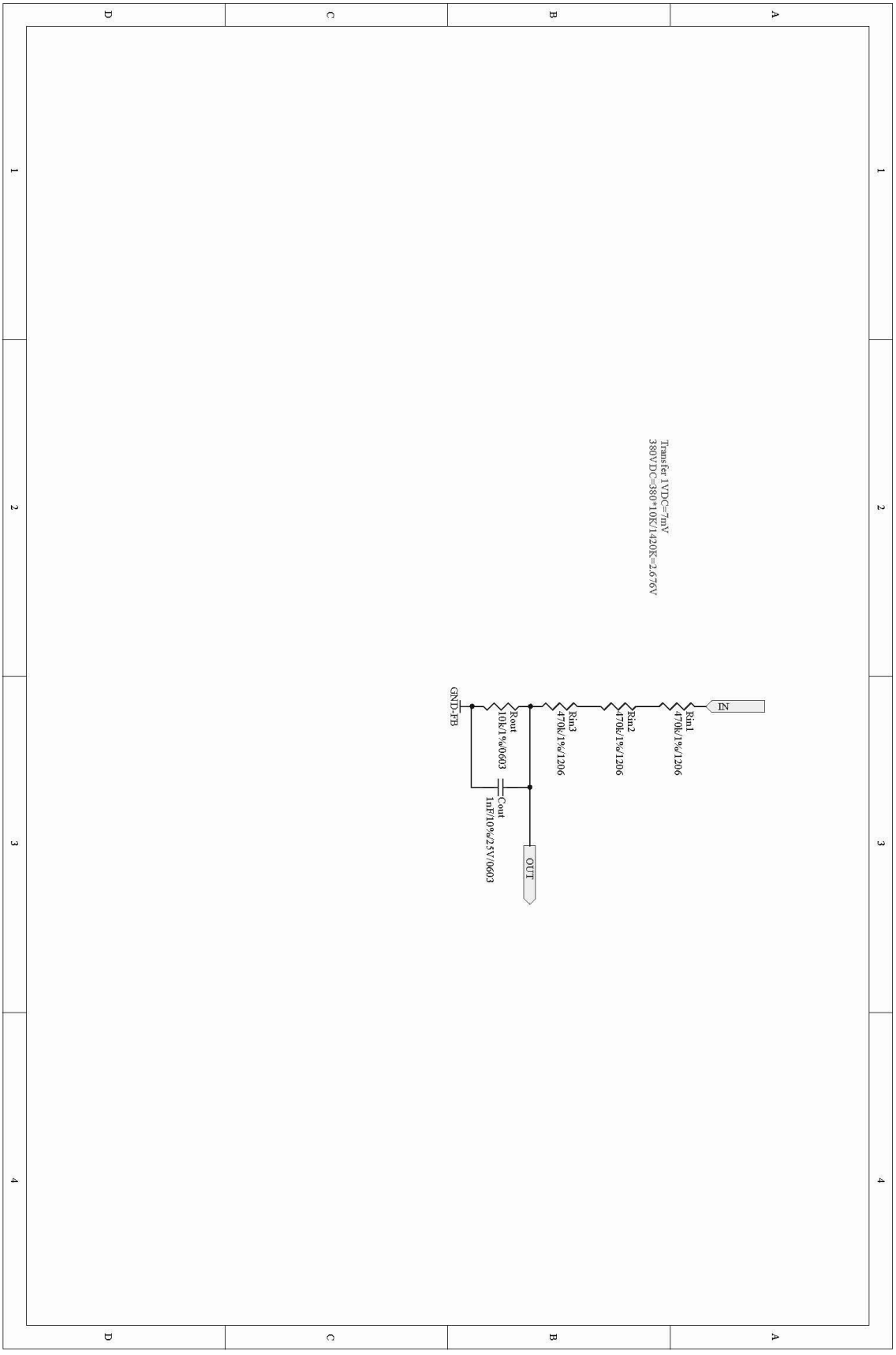

IN
Rin
100R/1%/0603
GND-FB
Cin
1nF/10%/25V/0603
FAN73711MX
GND
NC
NC
IN
VS
HO
VB
VDD
Cdc
1uF/10%/50V/0805
15V_FB
Rbst
5.1R/1206
Dbst
HS1M
Cgd
100nF/25V
1uF/10%/50V/0805
Cbst
Ebst
Emitter
Roff
100R/1206
SOD323-SH
Doff
Ron
22R/1206
BLM31PG121SZ1L
FBout
100pF/10%/25V/0603
Emitter
Rout
33k/1%/0603
Cout
E
G

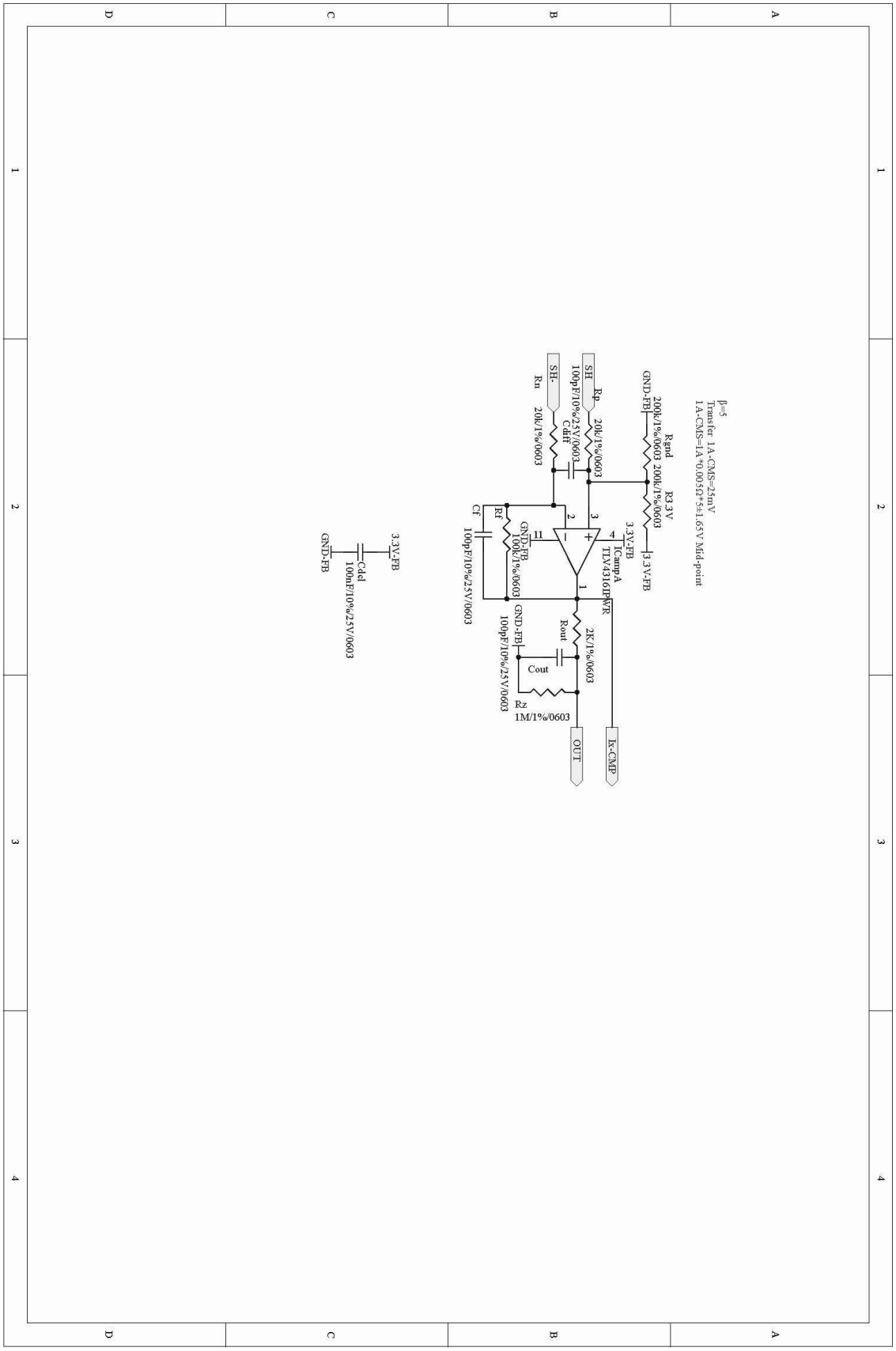

D
C
B
A
1
2
3
4
Sh+
GND-FB
2.2nF/10%/25V/0603
Rshp
470R/1%/0603
Ccmp
Sh-
GND-FB
2.2nF/10%/25V/0603
Rshn
470R/1%/0603
Ccmn
Cdm
2.2nF/10%/25V/0603
CS+
CS-

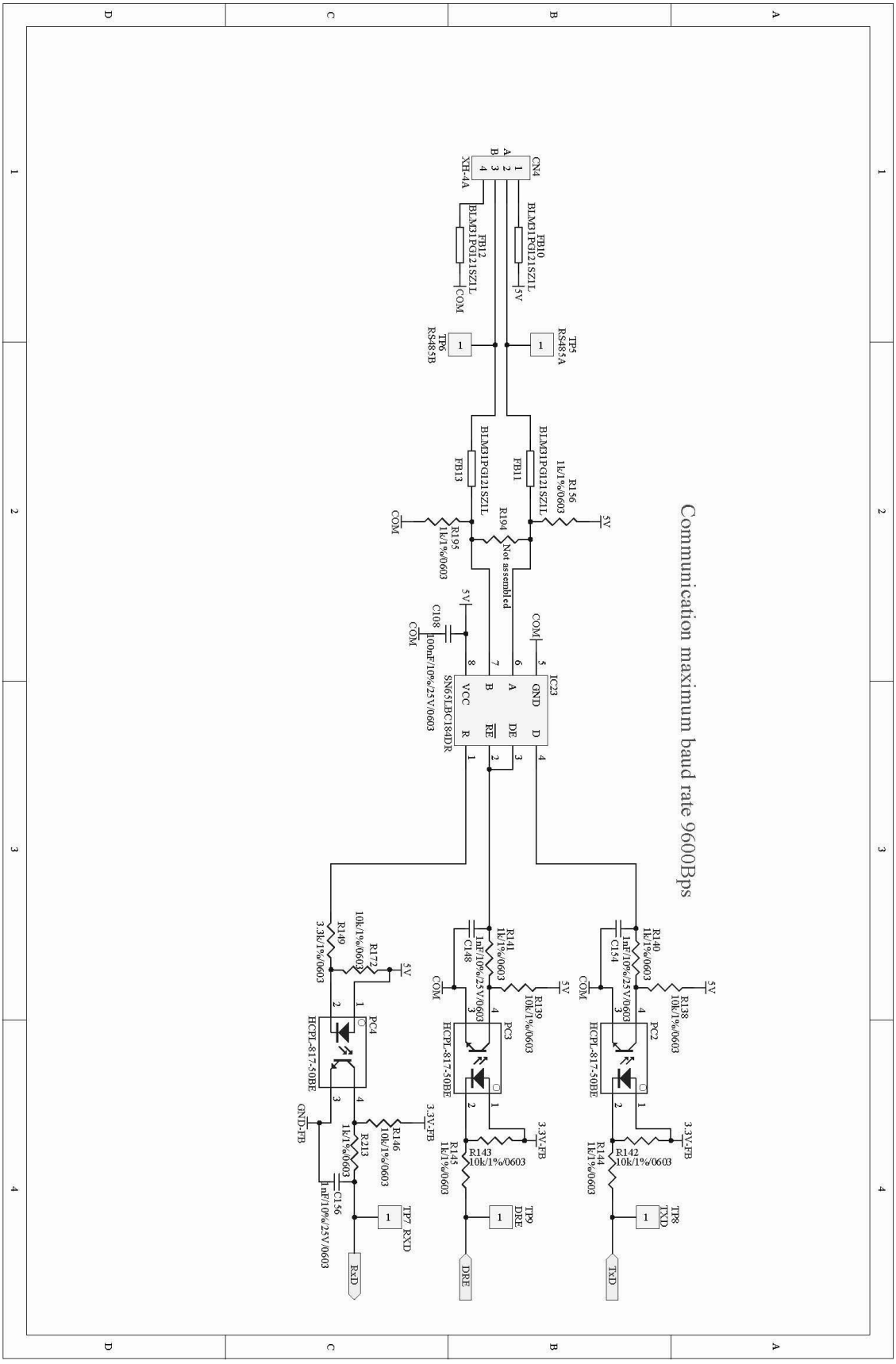

JTAG test reset
Device Reset
PTC-CON
U24
TMS320F28027FPTT
PFC1-SHUNT
PFC2-SHUNT
PFC3-SHUNT
IU-SHUNT
IV-SHUNT
IW-SHUNT
DCP
Ik-CMP
Vout
Output
Designator
Analog.SchDoc
PIM-TEMP
PFC-EN
VDC
U_Communication
Communication.SchDoc
TxD
RxD
DRE
EEPROM
IC24
BR24T256FVT-W
CT1
CSTCE10M0G15C99-R0
R103
1M/1%/0603
R199
1k/1%/0603
R301
2.2k/1%/0603
C110
100nF/10%/25V/0603
C113
100nF/10%/25V/0603
C114
100nF/10%/25V/0603
C115
2.2uF/10%/16V/0603
C117
2.2uF/10%/16V/0603
C119
2.2uF/10%/16V/0603
C122
2.2uF/10%/16V/0603
R170
1K/1%/0603
R184
10k/1%/0603
R162
10k/1%/0603
R197
4.7k/1%/0603
R302
4.7k/1%/0603
LED1
SML-D13FW
GREEN
CN3
XH-4A
CN5
2.54 pitch double row pin header
Harness
GateSignals
INV-FAULT
VDC-FAULT
RST
DSB-PFC
GND-FB
3.3V-FB
TEST
SDA
CLK

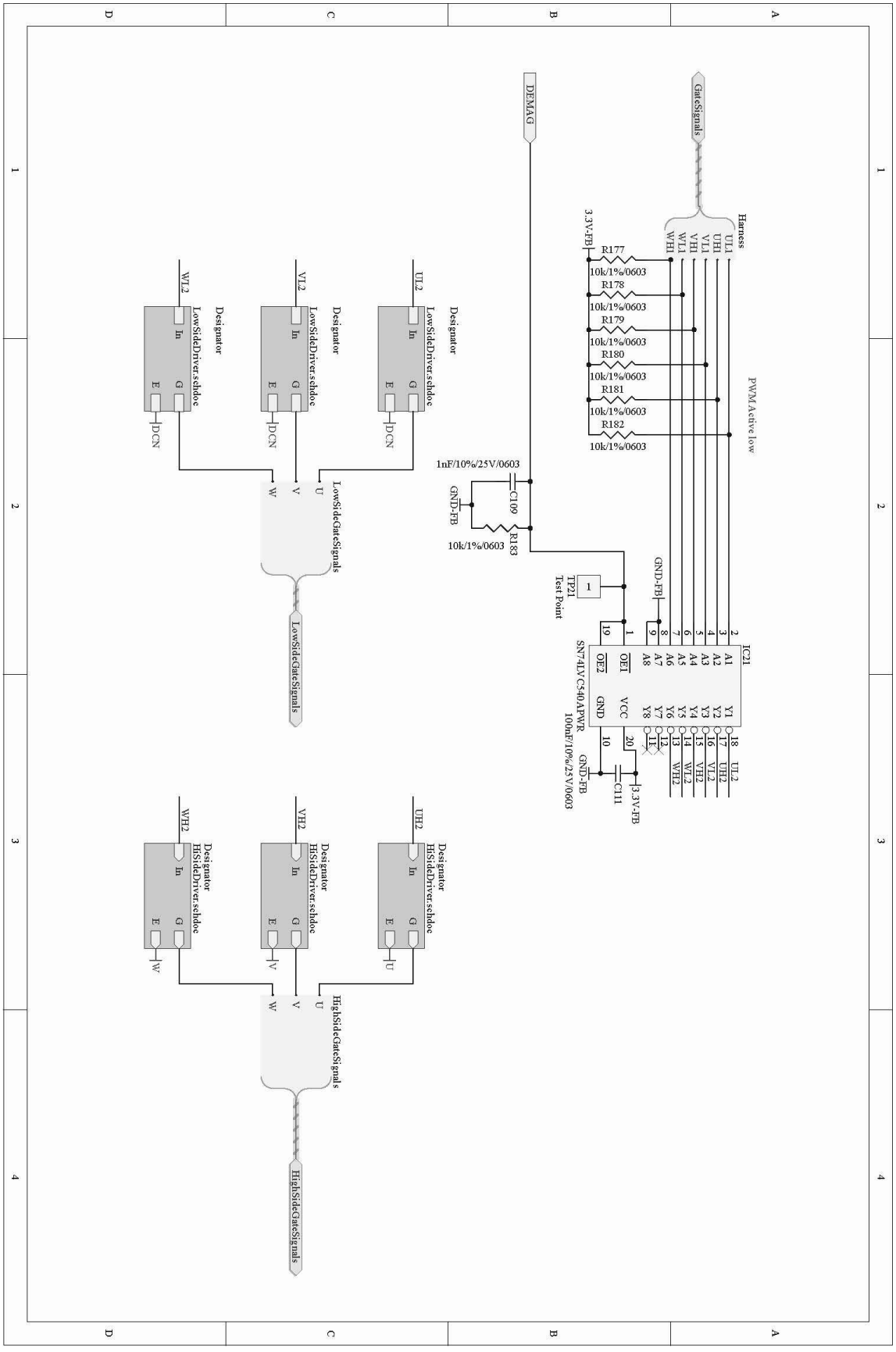

PFC Current sampling, software for unbalance detection
Transfer 1A-CMS=50mV
1A-CMS=1A*0.0051Ω*10+1.65V mid-point
β=5
PFC1-SHUNT
PFC2-SHUNT
PFC3-SHUNT
IU-SHUNT
IV-SHUNT
IW-SHUNT
Designator PfcCurrentMeas.schdoc
Designator InvCurrentMeas.schdoc
IPFC1
IPFC2
IPFC3
IU
IV
IW
Ix-CMP
IW-CMP
IV-CMP
IU-CMP
TP12 IPFC1
TP13 IPFC2
TP14 IPFC3
TP22 IU
TP23 IV
TP24 IW
Voltage Measurement
Designator OutputDevider.schDoc
VOUT-U
VOUT-V
VOUT-W
TP15 VOUT-U
TP16 VOUT-V
TP17 VOUT-W
220V-RMS=220*1.414*5/1430+1.65V mid-point
β=5/1430 Cutoff frequency=113Hz
Transfer 1V-CMS=3.5mV
AC-L
AC-N
VAC
TP26 Test Point
R71 470k/1%/1206
R75 470k/1%/1206
R72 470k/1%/1206
R83 20k/1%/0603
R70 10k/1%/0603
R73 20k/1%/0603
R74 20k/1%/0603
R81 470k/1%/1206
R78 470k/1%/1206
R79 470k/1%/1206
R82 20k/1%/0603
R84 10k/1%/0603
R86 10k/1%/0603
R80 2K/1%/0603
R85 1M/1%/0603
C60 1nF/10%/25V/0603
C67 100pF/10%/25V/0603
C62 1nF/10%/25V/0603
C64 100pF/10%/25V/0603
C63 100pF/10%/25V/0603
D18 LISS355T1G
D19 LISS355T1G
IC11B TLV2316IPWR
GND-FB
3.3V-FB
DCP
R69 20k/1%/0603
R243 470k/1%/1206
R68 470k/1%/1206
R67 470k/1%/1206
R255 20k/1%/0603
C146 100pF/10%/25V/0603
D21 LISS355T1G
IC15D TLV4316IPWR
R252 2K/1%/0603
C149 100pF/10%/25V/0603
R256 1M/1%/0603
TP25 Test Point
VDC
Transfer 1VDC=7mV
380VDC=380*10K/1420K=2.676V
IC19A TLV4316IPWR
C77 100nF/10%/25V/0603
IC11A TLV2316IPWR
C65 100nF/10%/25V/0603

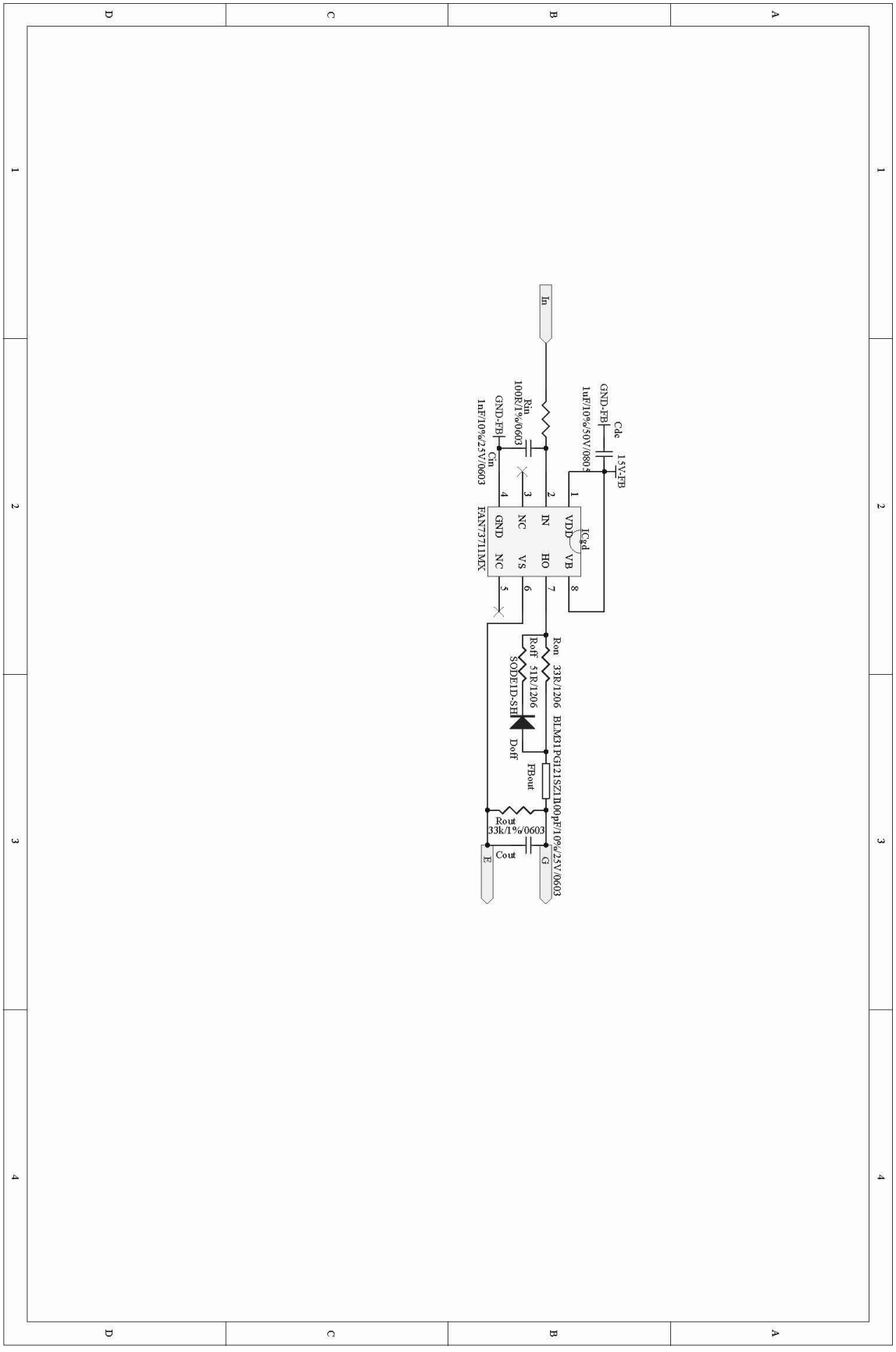

Transfer 1A-CMS=50mV
1A-CMS=1A*0.005Ω*10+1.65V mid-point
PFC Current sampling, software for unbalance detection
SH-
SH
GND-FB
200k/1%/0603
Rgnd
R3.3 V
200k/1%/0603
3.3V-FB
10k/1%/0603
Rp
100pF/10%/25V/0603
Cdiff
10k/1%/0603
Rn
6
5
7
CF
100pF/10%/25V/0603
Rf 100k/1%/0603
TLV4316IPWR
ICoaB
2K/1%/0603
Rout
GND-FB
100pF/10%/25V/0603
Cout
Rz
1M/1%/0603
OUT

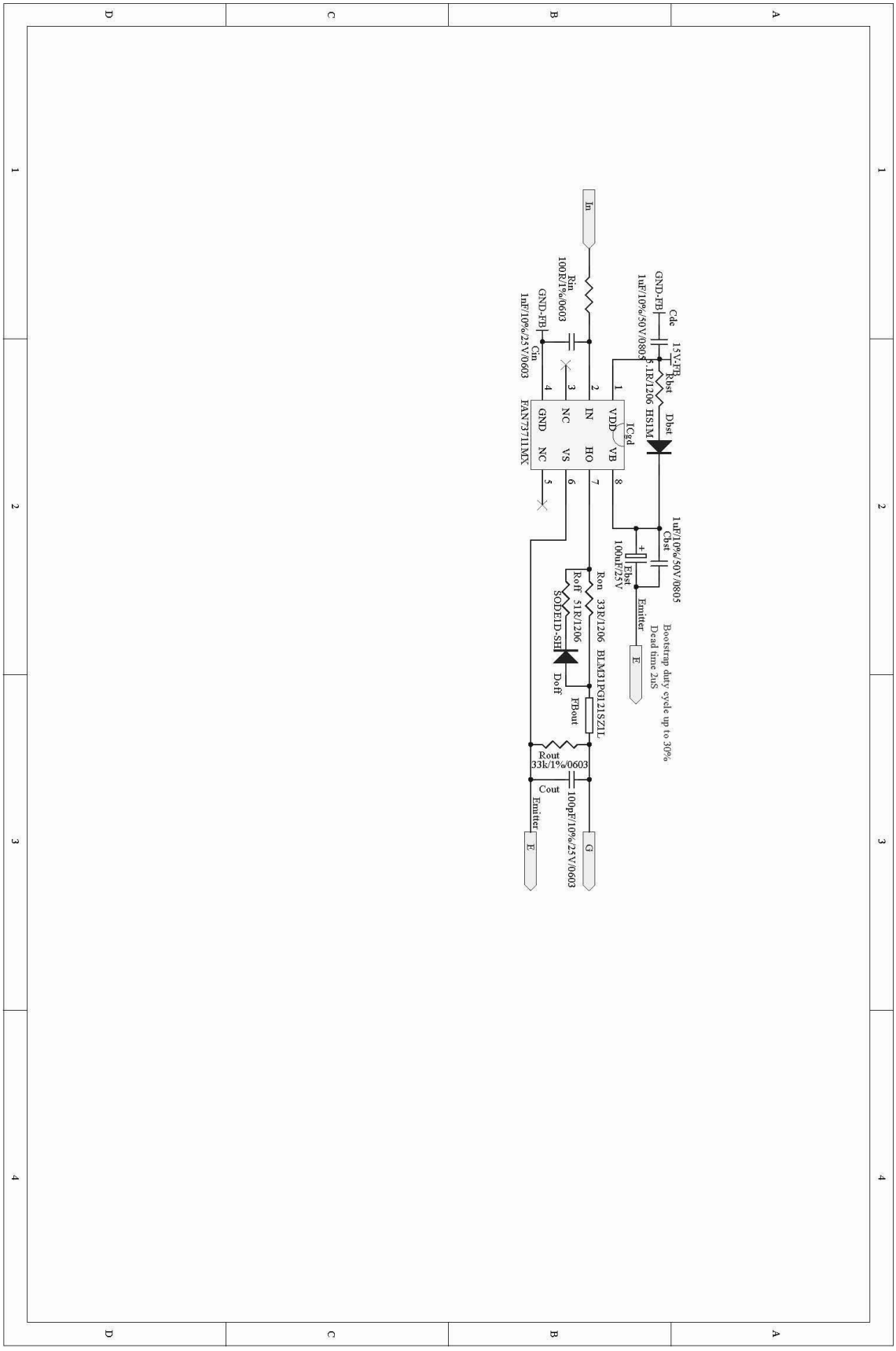

Transfer 1VDC=7mV
380VDC=380*10K/142OK=2.676V
IN
Rin1
470k/1%/1206
Rin2
470k/1%/1206
Rin3
470k/1%/1206
Rout
10k/1%/0603
Cout
1nF/10%/25V/0603
GND-FB
OUT

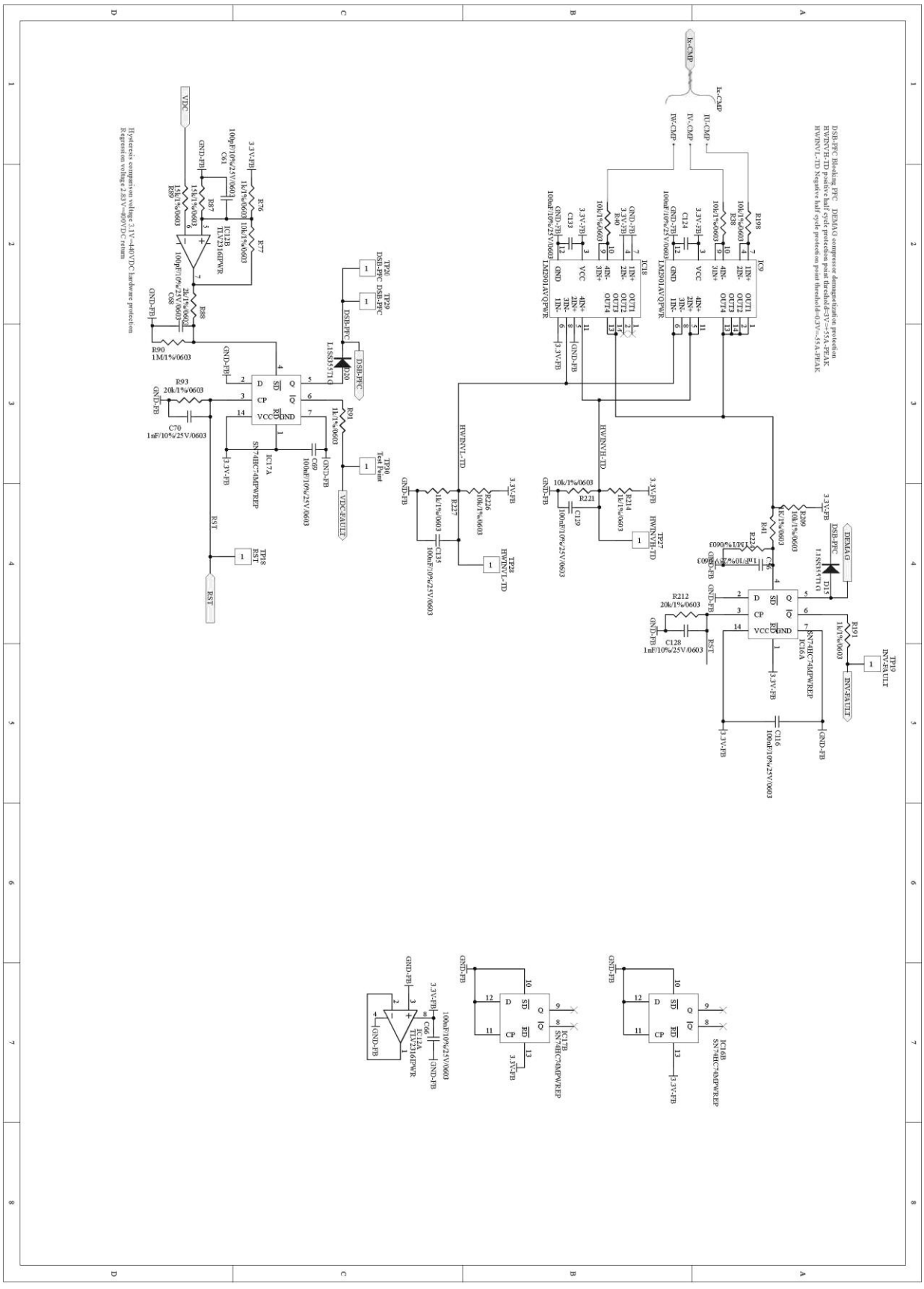

β=5
Transfer 1A-CMS=25mV
1A-CMS=1A*0.005Ω*5±1.65V Mid-point
Rgnd
200k/1%/0603
GND-FB
R3.3V
200k/1%/0603
3.3V-FB
SH-
Rn
20k/1%/0603
SH
Rp
20k/1%/0603
100pF/10%/25V/0603
Cdiff
Cf
100pF/10%/25V/0603
Rf
100k/1%/0603
GND-FB
11
2
3
4
1
3.3V-FB
IcompA
TLV4316IPWR
GND-FB
100pF/10%/25V/0603
Cout
Rout
2K/1%/0603
Rz
1M/1%/0603
OUT
Ix-CMP
3.3V-FB
Cdd
100nF/10%/25V/0603
GND-FB

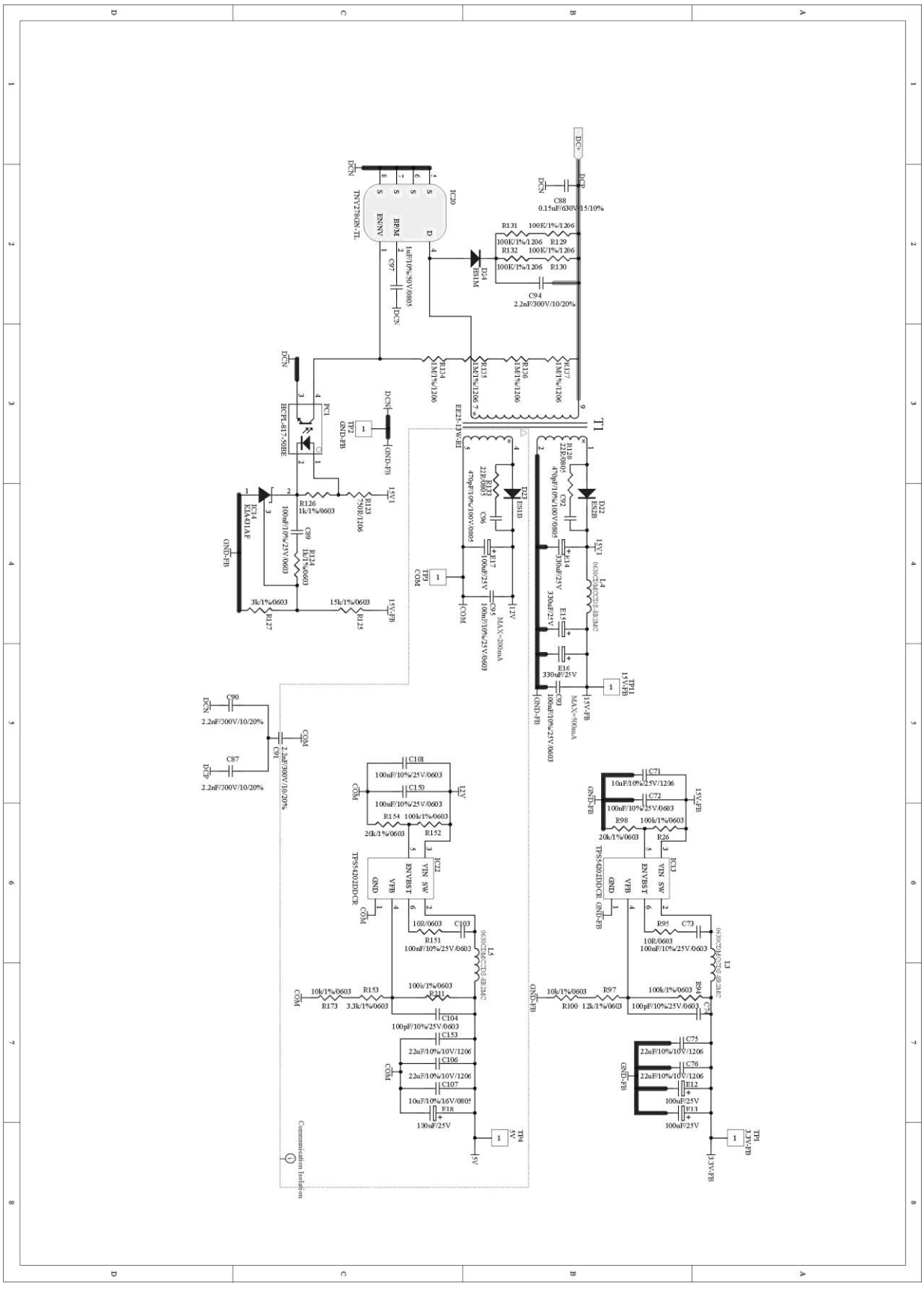

Communication maximum baud rate 9600Bps
CN4
XH-4A
FB12
BLM31PG121SZ1L
FB10
BLM31PG121SZ1L
TP6
RS485B
TP5
RS485A
FB13
FB11
R156
1k/1%/0603
R194
Not assembled
R195
1k/1%/0603
C108
100nF/10%/25V/0603
IC23
SN65LBC184DR
R140
1k/1%/0603
C154
1nF/10%/25V/0603
R138
10k/1%/0603
PC2
HCPL-817-50BE
R141
1k/1%/0603
C148
1nF/10%/25V/0603
R139
10k/1%/0603
PC3
HCPL-817-50BE
R149
3.3k/1%/0603
R172
10k/1%/0603
PC4
HCPL-817-50BE
R213
1k/1%/0603
C156
1nF/10%/25V/0603
R146
10k/1%/0603
R142
10k/1%/0603
R144
1k/1%/0603
R143
10k/1%/0603
R145
1k/1%/0603
TP7 RXD
TP8 TXD
TP9 DRE
RxD
TxD
DRE
5V
COM
3.3V-FB
GND-FB


GateSignals
Harness
UL1
UH1
VL1
VH1
WL1
WH1
PWMActive low
3.3V-FB
R177
10k/1%/0603
R178
10k/1%/0603
R179
10k/1%/0603
R180
10k/1%/0603
R181
10k/1%/0603
R182
10k/1%/0603
DEMAG
1nF/10%/25V/0603
C109
GND-FB
R183
10k/1%/0603
TP21
Test Point
GND-FB
IC21
SN74LVC540APWR
OE1
OE2
VCC
GND
A1
A2
A3
A4
A5
A6
A7
A8
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
100nF/10%/25V/0603
C111
3.3V-FB
UL2
VL2
WL2
UH2
VH2
WH2
Designator
LowSideDriver.schdoc
HiSideDriver.schdoc
In
E
G
DCN
U
V
W
LowSideGateSignals
HighSideGateSignals


In
Cdc
GND-FB
1uF/10%/50V/0805
15V-FB
Rin
100R/1%/0603
Cin
GND-FB
1nF/10%/25V/0603
FAN7711MX
GND
NC
NC
VS
HO
VB
IN
VDD
ICgd
Ron
33R/1206
Roff
51R/1206
SOD1E1D-SH
Doff
FBout
BLM31PG121SZ1L
100pF/10%/25V/0603
Rout
33k/1%/0603
Cout
E
G


In
Rin
100R/1%/0603
GND-FB
Cin
1nF/10%/25V/0603
FAN7711MX
GND
NC
NC
VS
HO
VB
IN
VDD
ICgd
Cdc
GND-FB
1uF/10%/50V/0805
15V-FB
Rbst
5.1R/1206
Dbst
HS1M
1uF/10%/50V/0805
Cbst
Ebst
100uF/25V
Emitter
E
Bootstrap duty cycle up to 30%
Dead time 2uS
Ron
33R/1206
BLM31PG121SZ1L
Roff
51R/1206
SOD1D-SH
Doff
FBout
Rout
33k/1%/0603
Cout
100pF/10%/25V/0603
Emitter
E
G


Ic-CMP
IW-CMP
IV-CMP
IU-CMP
DSB-PFC Blocking PFC DEMAG compressor demagnetization protection
HWINVH-TD positive half cycle protection point threshold=3V~~55A-PEAK
HWINVL-TD Negative half cycle protection point threshold=0.3V~~55A-PEAK
VDC
Hysteresis comparison voltage:3.1V~~400VDC hardware protection
Regression voltage:2.85V~~400VDC return
DSB-PFC
DEMAG
INV-FAULT
RST
HWINVH-TD
HWINVL-TD
VDC-FAULT


DC+
DCN
DCP
IC20
TNY278GN-TL
C88
0.15uF/630V/15/10%
R131 100K/1%/1206
R132 100K/1%/1206
R129 100K/1%/1206
R130 100K/1%/1206
D24
HS1M
C94
2.2nF/300V/10/20%
C97
1nF/10%/50V/0805
R114 1M/1%/1206
R115 1M/1%/1206
R116 1M/1%/1206
R117 1M/1%/1206
T1
EE22-13W-RL
FC1
HCPL-817-500E
TP2
GND-FB
R126 11k/1%/0603
R123 150R/1206
D21
ES1AF
C89 100nF/10%/25V/0603
R124 1E/1%/0603
R127 3k/1%/0603
R125 15k/1%/0603
15V-FB
12V
R128 22R/0805
C92 470pF/10%/100V/0805
D23 ES1D
C96
E17 100uF/25V
C95 100nF/10%/25V/0603
MAX=300mA
D22 ES2B
E14 330uF/25V
E15
E16 330uF/25V
C93 100nF/10%/25V/0603
MAX=500mA
TP1
15V-FB
TP3
COM
C90 2.2nF/300V/10/20%
C87 2.2nF/300V/10/20%
C91 2.2nF/300V/10/20%
C101 100nF/10%/25V/0603
C159 100nF/10%/25V/0603
R154 20k/1%/0603
R152 100k/1%/0603
IC22
TPS54202DDCR
VIN SW
EN VBST
GND VFB
R151 10R/0603
C103 100nF/10%/25V/0603
L5
R153 10k/1%/0603
R173 3.3k/1%/0603
R211 100k/1%/0603
C104 100pF/10%/25V/0603
C153 22uF/10%/10V/1206
C106 22uF/10%/10V/1206
C107 10uF/10%/16V/0805
E18 100uF/25V
TP4
5V
Communication Isolation
C71 10uF/10%/25V/1206
C72 100nF/10%/25V/0603
R98 20k/1%/0603
R26 100k/1%/0603
IC3
TPS54202DDCR
R95 10R/0603
C73 100nF/10%/25V/0603
L3
R100 12k/1%/0603
R97 10k/1%/0603
R94 100k/1%/0603
C74 100pF/10%/25V/0603
C75 22uF/10%/10V/1206
C76 22uF/10%/10V/1206
E12 100uF/25V
E13 100uF/25V
TP5
3.3V-FB

7 Hardware description

The following section gives a description of the hardware.

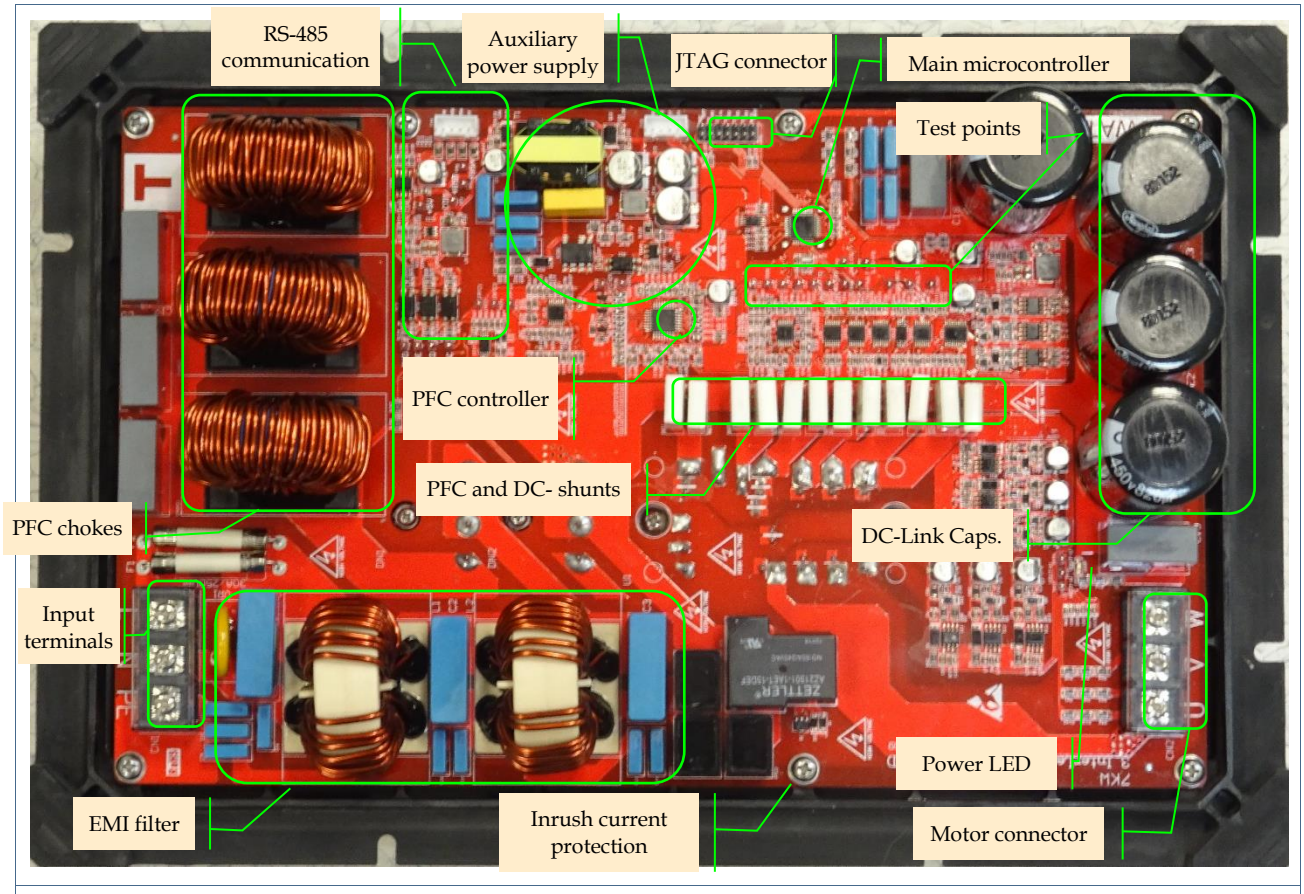


Figure 4: The EVA board

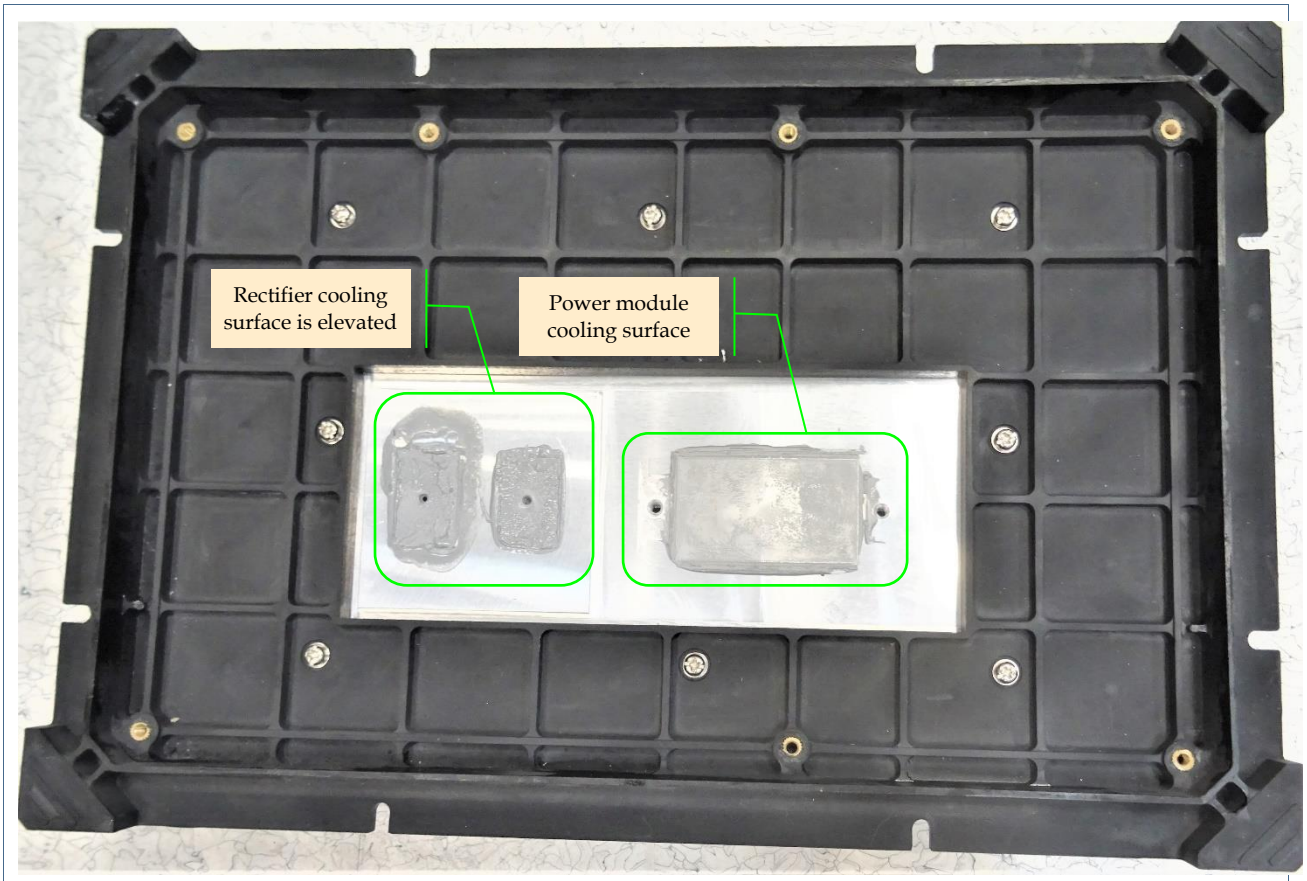
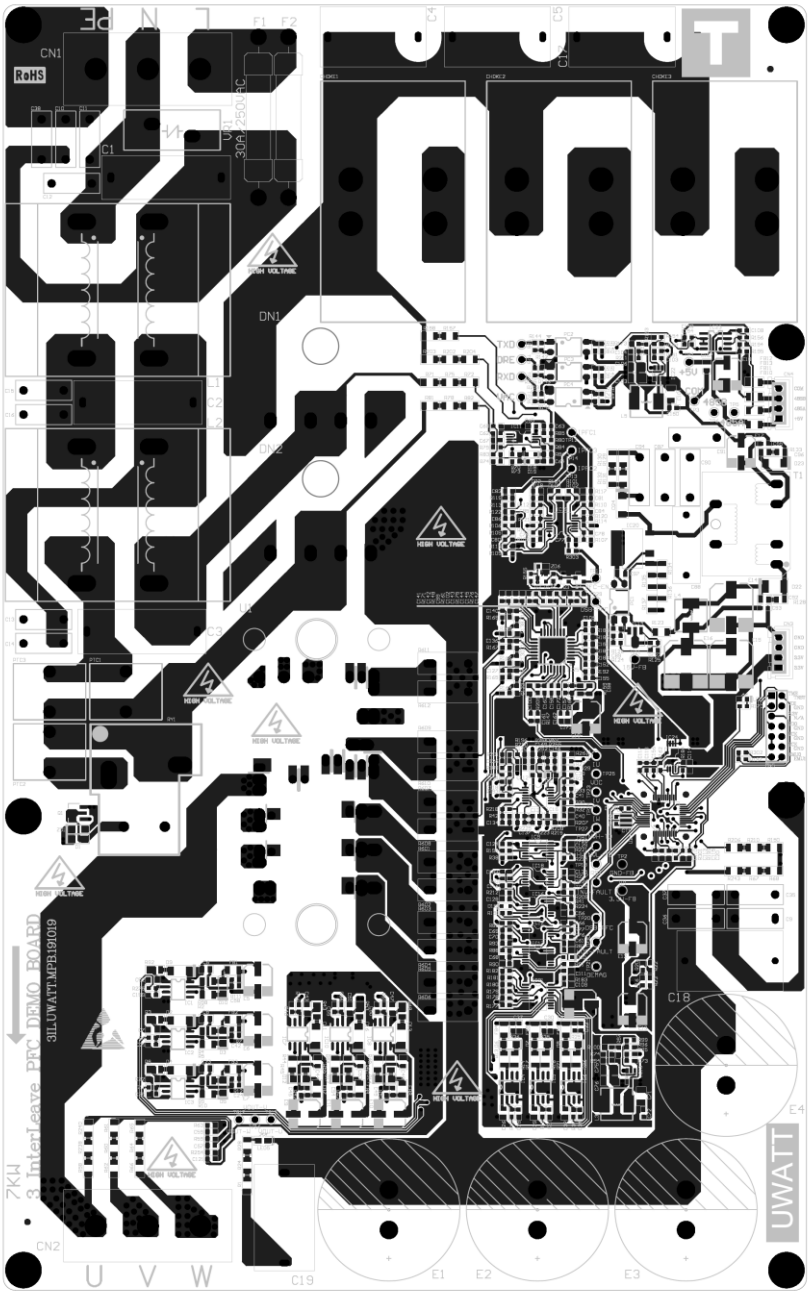


Figure 5: The hole profile and heatsink design

7.1 Dimensions and Board Layout

The board dimensions are 320 mm x 200 mm with four layers of 2 oz copper (70 µm) and an insulator thickness of min 2 mm.



				Document No.	3IL.UWATT.MPB.191019				TG temperature class:	140
				verson No.	V03	Material: Four layer epoxy board	Plate thickness	2mm ± 0.1mm		CTI: ≥600V
						Technology: Lead-free HASL	Base copper thickness:	2oZ (70uM ± 10%)		RoHS compliant
						Screen printing color: white	Flame retardant grade:	UL94V - 0 FR-4		Plate color: Red

Technical requirement:
1. All pads are made according to PTH 2. The minimum line width / line distance processing capacity meets the requirements of 8mil
3. PTH copper wall thickness of vias and pads shall be no less than 20um without special requirements; 4. For all via with hole size = 0.5mm, make oil cover for via

Figure 6: Top layer and overlay

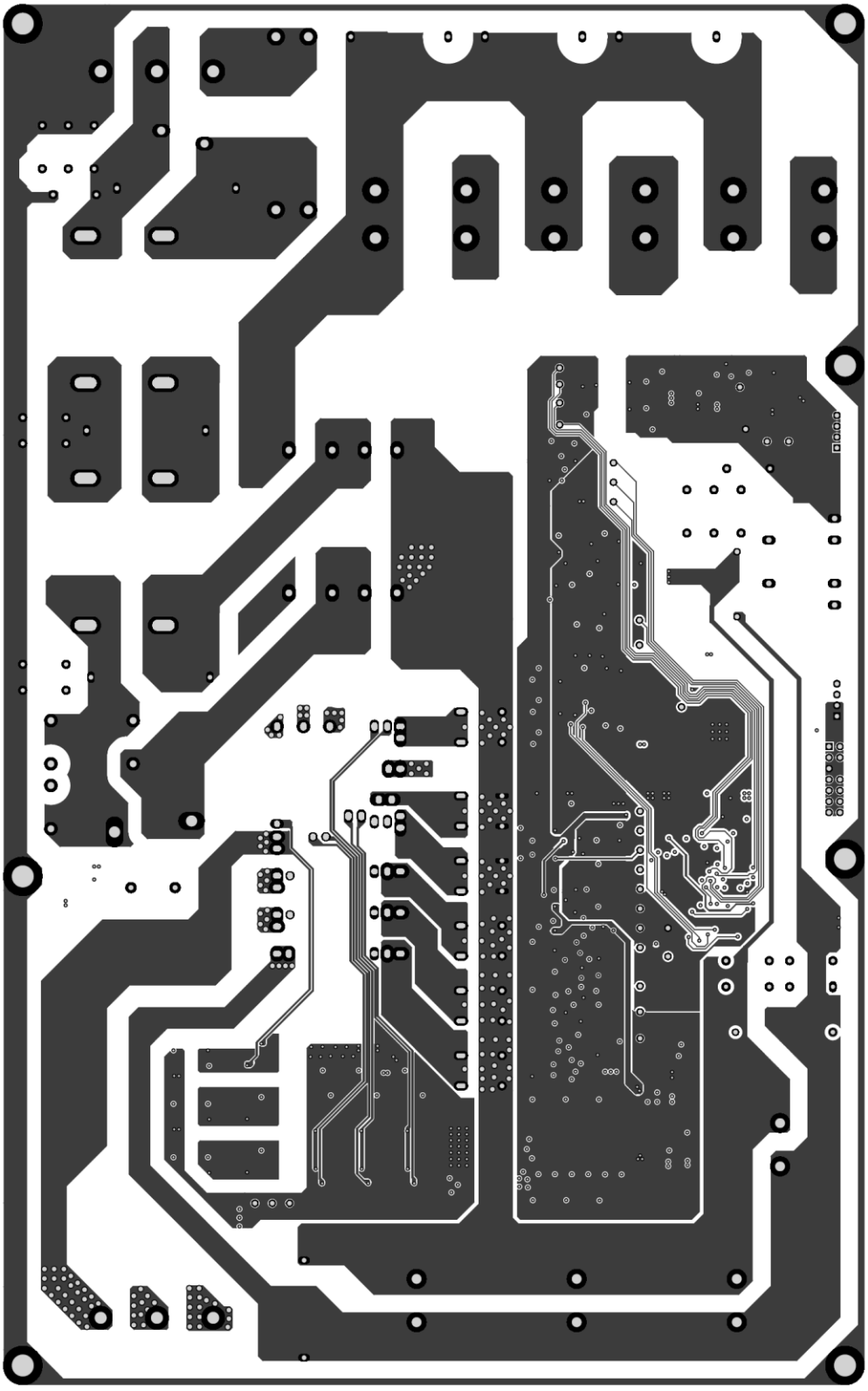


Figure 7: Mid1 layer

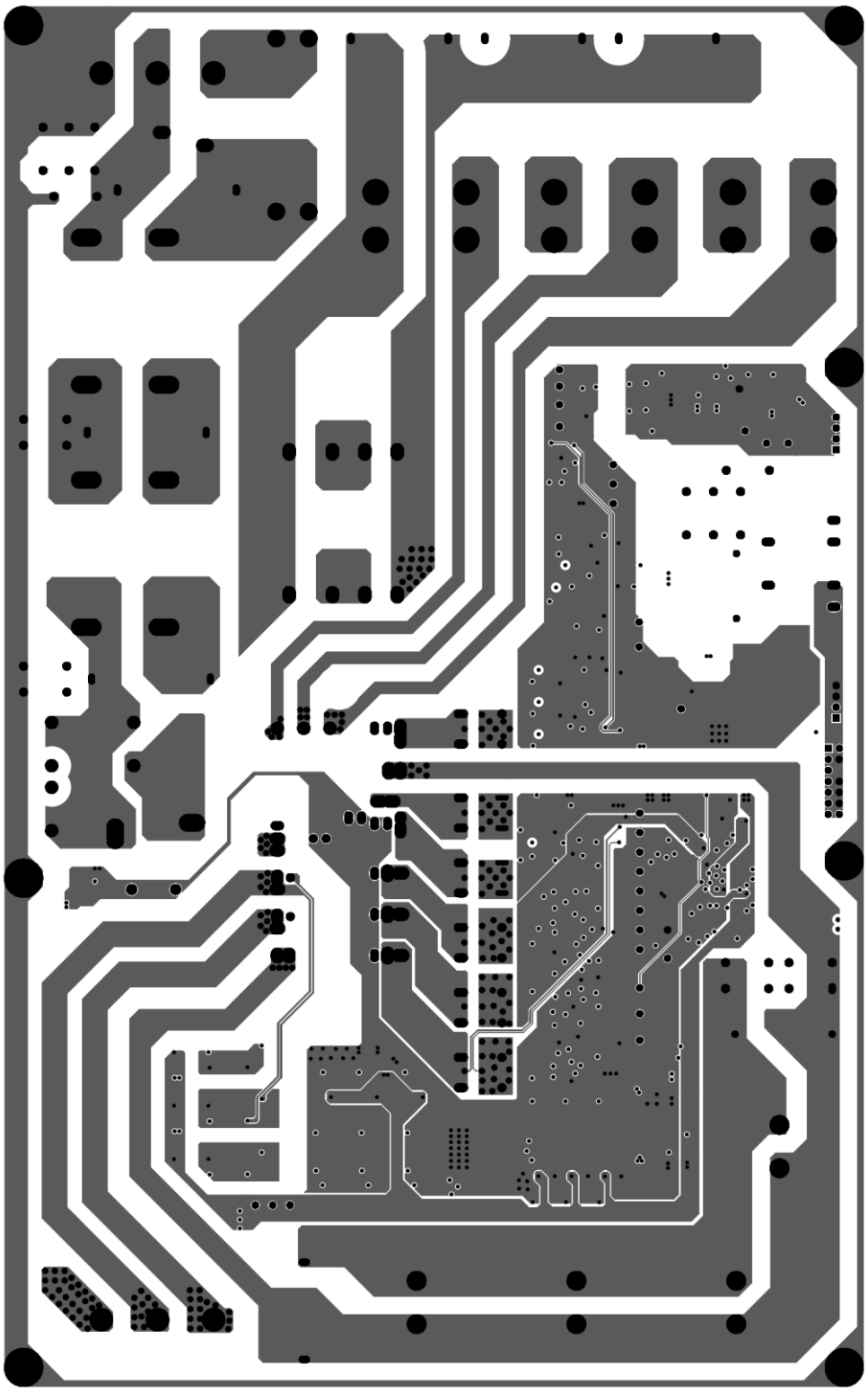


Figure 8: Mid2 layer

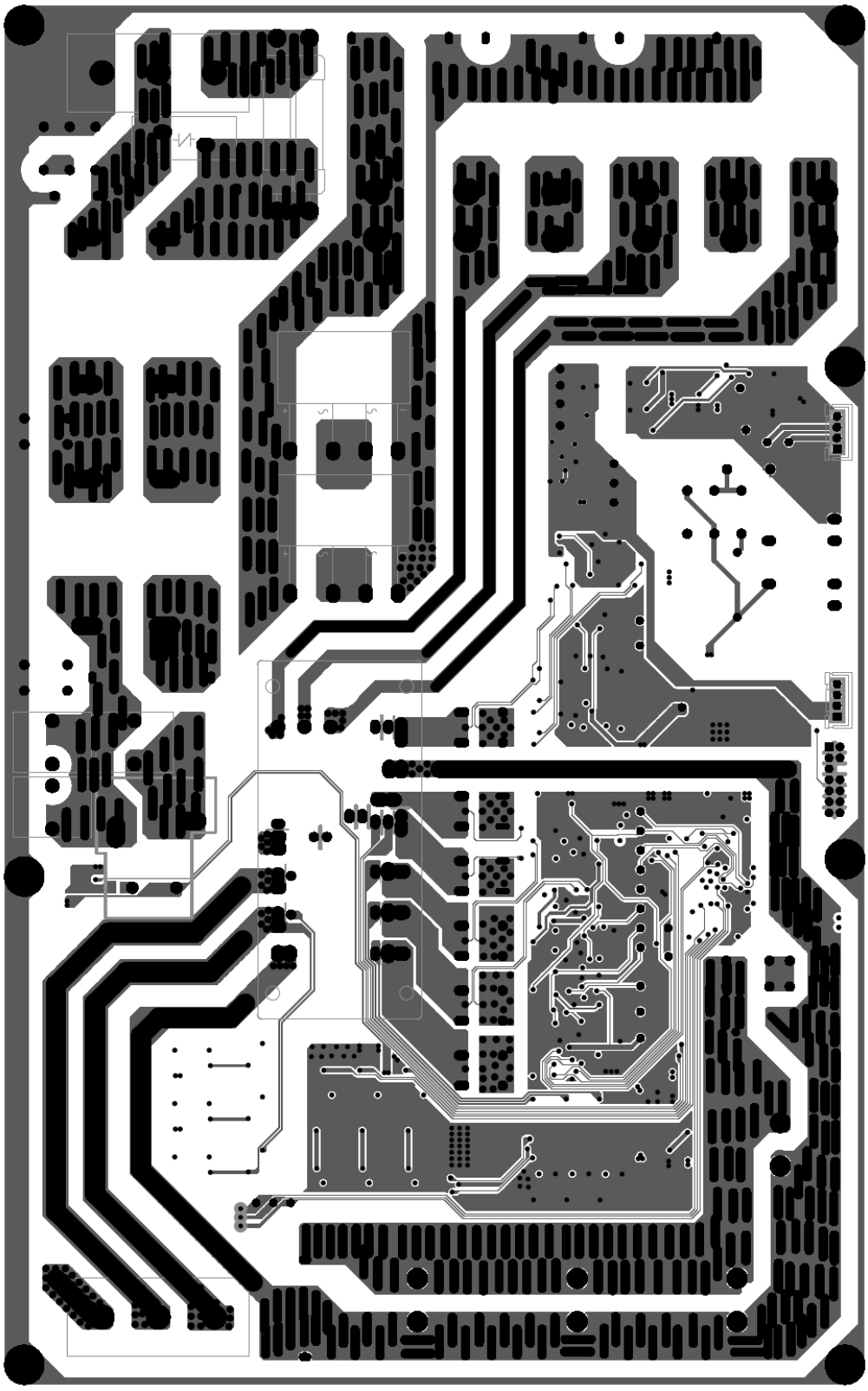


Figure 9: Bottom layer and overlay

8 BOM

Item	Name	Brand	Type	Parameter	Reference	Qty
1	Power Module	VINCOTECH	10-PG06PPA050SJ02-LH94E08T	50A/600V power module, PFC-INV	U1	1
2	Res_SMD	Yageo	1206	470k/1%/1206	R1, R24, R28, R58, R60, R61, R62, R64, R65, R66, R67, R68, R71, R72, R75, R78, R81, R82, R238, R240, R243	21
3	Res_SMD	Yageo	0603	100R/1%/0603	R6, R11, R15, R19, R37, R46, R51, R56, R275	9
4	Res_SMD	Yageo	0603	33k/1%/0603	R7, R12, R25, R34, R35, R47, R52, R57, R111	9
5	Res_SMD	Yageo	0603	47R/1%/0603	R16	1
6	Res_SMD	Yageo	0603	100k/1%/0603	R20, R33, R94, R96, R152, R201, R211, R225	8
7	Res_SMD	Yageo	0603	1k/1%/0603	R22, R41, R76, R91, R124, R126, R140, R141, R144, R145, R156, R170, R191, R195, R199, R213, R214, R227,R303	19
8	Res_SMD	Yageo	0603	10k/1%/0603	R23, R38, R40, R59, R63, R70, R77, R84, R86, R100, R120, R121, R122,R138, R139, R142, R143, R146, R155, R162, R172, R173, R174, R177, R178, R179, R180, R181, R182, R183, R184, R198, R209, R221, R226, R254,R185	37
9	Res_SMD	Yageo	0603	200k/1%/0603	R26, R27, R189, R190, R207, R208	6
10	Res_SMD	Yageo	0603	20k/1%/0603	R29, R31, R39, R69, R73, R74, R79, R83, R93, R99, R101, R102, R103, R104,	23

					R105, R106,R154, R187, R193, R212, R215, R223, R255	
11	Res_SMD	Yageo	0603	2K/1%/0603	R30, R80, R88, R107,R108,R109,R110, R112, R113,R114, R115, R116, R196, R218, R252	15
12	Res_SMD	Yageo	0603	1M/1%/0603	R32, R42, R85, R90, R117, R118, R119, R163, R200, R224, R256	11
13	Res_SMD	Yageo	0603	15k/1%/0603	R87, R89, R125	3
14	Res_SMD	Yageo	0603	12k/1%/0603	R97, R186	2
15	Res_SMD	Yageo	0603	3k/1%/0603	R127	1
16	Res_SMD	Yageo	1206	100K/1%/1206	R129, R130, R131, R132	4
17	Res_SMD	Yageo	1206	1M/1%/1206	R134, R135, R136, R137, R150, R157, R158, R206, R210	9
18	Res_SMD	Yageo	0603	19.6k/1%/0603	R147	1
19	Res_SMD	Yageo	0603	470k/1%/0603	R148	1
20	Res_SMD	Yageo	0603	3.3k/1%/0603	R149, R153	2
21	Res_SMD	Yageo	0805	200k/1%/0805	R159	1
22	Res_SMD	Yageo	0603	16.2k/1%/0603	R160	1
23	Res_SMD	Yageo	0603	75k/1%/0603	R161, R175, R176	3
24	Res_SMD	Yageo	0603	470R/1%/0603	R164, R165, R166, R167, R168, R169	6
25	Res_SMD	Yageo	0603	36K/1%/0603	R171,R192	2
26	Res_SMD	Yageo	0603	39K/1%/0603	R188	1
27	Res_SMD	Yageo	N/A	Not assembled	R194	1
28	Res_SMD	Yageo	0603	4.7k/1%/0603	R197, R302,R205	3

29	Res_SMD	Yageo	1206	4.02M/1%/1206	R202, R203, R204	3
30	Res_SMD	Yageo	0603	2.2k/1%/0603	R301	1
31	Res_SMD	Yageo	1206	51R/1206	R2, R5, R10, R14, R18, R36	6
32	Res_SMD	Yageo	1206	5.1R/1206	R3, R8, R43, R48, R53, R92	6
33	Res_SMD	Yageo	1206	33R/1206	R4, R9, R13, R17, R21, R98	6
34	Res_SMD	Yageo	1206	22R/1206	R44, R49, R54	3
35	Res_SMD	Yageo	1206	100R/1206	R45, R50, R55	3
36	Res_SMD	Yageo	0603	10R/0603	R95, R151	2
37	Res_SMD	Yageo	1206	750R/1206	R123	1
38	Res_SMD	Yageo	0805	22R/0805	R128, R133	2
39	Cap_SMD	MURATA	0603	47pF/10%/100V/ 0603/X7R	C118,C126,C131,C137,C39, C41	6
40	Cap_SMD	MURATA	0805	470pF/10%/100V /0805/X7R	C92, C96	2
41	Cap_SMD	MURATA	0805	47nF/10%/100V/ 0805/X7R	C98	1
42	Cap_SMD	MURATA	0603	470pF/10%/200V /0603/X7R	C141,C152, C161	3
43	Cap_SMD	MURATA	0603	100nF/10%/50V/ 0603/X7R	C20, C65, C66, C69, C72, C73, C77, C89, C93, C95, C103, C108, C110, C111, C112, C113, C114, C116, C124, C129, C133, C135, C150, C162,C160	25
44	Cap_SMD	MURATA	0603	1nF/10%/50V/06 03/C0G	C56, C57, C59, C60, C62, C70, C109, C121, C128, C142, C148, C154, C156,C172	14
45	Cap_SMD	MURATA	0603	100pF/10%/50V/ 0603/C0G	C24, C27, C30, C33,C40, C42, C45, C49, C54, C58, C61, C63, C64, C67, C68, C74, C78, C79, C80, C81, C82, C83, C84, C85, C86,	36

					C104,C120, C134,C146, C149, C99, C143, C145, C102,C144,C147	
46	Cap_SMD	MURATA	0805	1uF/10%/50V/0805/X7R	C6, C7, C8, C22, C23, C26, C29, C32, C43, C44, C47, C48, C51, C52, C53, C97,C100	17
47	Cap_SMD	MURATA	1206	10uF/10%/25V/1206/X7R	C71, C101	2
48	Cap_SMD	MURATA	1206	22uF/10%/10V/1206/X7R	C75, C76, C106, C153	4
49	Cap_SMD	MURATA	0603	10nF/10%/100V/0603/X7R	C105, C151, C155	3
50	Cap_SMD	MURATA	0805	10uF/10%/16V/0805/X7S	C107	1
51	Cap_SMD	MURATA	0603	2.2uF/10%/16V/0603/X7S	C115, C117, C119, C122, C171, C158	6
52	Cap_SMD	MURATA	0603	2.2nF/10%/100V/0603/X7R	C123, C125, C127, C130, C132, C136, C138, C139, C140	9
53	Cap_SMD	MURATA	0603	470nF/10%/25V/0603/X7R	C157	1
54	X2 Cap	EPCOS	B32934B3105K	1uF/305V/27.5/10%	C1, C2, C3	3
55	Film Capacitor	EPCOS	B32673Z6225	2.2uF/630V/22.5/10%	C4, C5, C17, C18, C19	5
56	Y2 Cap	EPCOS	B32021A3222M	2.2nF/300V/10/20%	C9, C10, C11, C12, C13, C14, C15, C16, C35, C36, C37, C38, C87, C90, C91, C94	16
57	Film Cap	EPCOS	B32672Z6154K	0.15uF/630V/15/10%	C88	1
58	Elec_Cap_SMD	RUBYCON	25TRV100M6.3X8	100uF/25V	E5, E6, E7, E8, E9, E10, E11, E12, E13, E17, E18, E19	12

59	Elec_Cap_SMD	RUBYCON	25TRV330M 10X10.5	330uF/25V	E14, E15, E16	3
60	Bead_SMD	MURATA	BLM31PG121SZ1L	120Ω/3500mA	FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB10, FB11, FB12, FB13	13
61	IC	ON	FAN73711MX	3A High-side driver	IC1, IC2, IC3, IC4, IC5, IC6, IC7, IC8, IC10	9
62	Comp	Ti	LM2901AVQPWR	4 Channel comparator	IC9, IC18	2
63	Amp.	Ti	TLV9062IPWR	Dual Operational Amplifier	IC11, IC12	2
64	Amp.	Ti	TLV4316IPWR	Quad Operational Amplifier	IC15, IC19	2
65	Amp.	Ti	SN74HC74MPWREP	D flip-flop	IC16, IC17	2
66	DC/DC	Ti	TPS54202DDCR	Synchronous rectifier	IC13, IC22	2
67	tristate logic inverter	Ti	SN74LVC540APWR	Octal Buffers with 3-State Outputs	IC21	1
68	485 Converter	Ti	SN65LBC184DR	485-232	IC23	1
69	EEPROM	Atmel	AT24C04B-TH-T	Memory	IC24	1
70	PFC Controller	ON	FAN9673Q	CCM-PFC Controller	IC25	1
71	IC	PI	TNY278GN-TL	Integrated MOS Off-Line Switcher	IC20	1
72	Inductor SMD	Onsemi	0630CDMCCDS-8R2MC	inductor	L3, L4, L5	3
73	LDO	KEC	KIA431AF	2.5V Precision voltage regulator	IC14	1
74	LED	ROHM	SML-D13FW	LED green 0603	LED1	1
75	LED	EVERLIGHT	17-21SURCS530-A3TR8	LED red 0805	LED5	1

76	Opto SMD	AVAGO	HCPL-817-50BE	5000VAC-817	PC1, PC2, PC3, PC4	4
77	Transistor SMD	ROHM	DTDG23YP	Digital transistor /SOT-89	Q1	1
78	Transistor SMD	KEC	KRC246S	Digital transistor /SOT-23	Q2, Q3, Q4	3
79	Relay	ZETTLER GROUP	AZ21501-1AET-15DEF	15VDC-50A Monostable	RY1	1
80	DSP	Ti	TMS320F28027FPTT	DSP	U24	1
81	TVS	LRC	SODJ16A-SH	TVS	ZD1	1
82	Zener Diode SMD	LRC	UDZ5V1BF	ZENER	ZD6	1
83	Diode SMD	DIODES	ES1B	100V/1A	D23	1
84	Diode SMD	DIODES	ES2B	100V/2A	D22	1
85	Diode SMD	LRC	L1SS355T1G	75/100mA/SOD-323	D15, D18, D19, D20, D21	5
86	Diode SMD	Good-ark	HS1M	1000V/1A/DO214A	D2, D4, D9, D11, D13, D16, D24	7
87	Diode SMD	LRC	SODE1D-SH	200V/1A/SOD-123	D1, D3, D5, D6, D7, D8, D10, D12, D14, D17	10
88	Rectifier Bridge	ShinDengen	D25XB80	25A/800V	DN1, DN2	2
89	Osc.	MURATA	CSTCE10M0G15C99-R0	10M	CT1	1
90	Varistor	Wurth	820423211	320VAC diameter 20mm	VR1	1
91	PTC	Dandong Guotong	MZ-100R	100Ω	PTC1, PTC2, PTC3	3
92	Fuse	Littlefuse	0325030MXP	250VAC/30A	F1, F2	2
93	Terminal	JST	XH-4A	4pin	CN3，CN4	2
94	Terminal	JITE	BTB750-01-3-1	Barrier terminal 3Pin	CN1, CN2	2

95	PFC Choke	Qingdao	RC20N15RJ	20A/150uH	CHOKE1, CHOKE2, CHOKE3	3
96	Pin_ DSP Programming	Generic	2.54 Double row		CN5 See note 1)	1
97	Common Mode Choke	Qingdao	LT38-4P-014/2.5mH-30A	30A/2.5mH	L1, L2	2
98	Transformer	Generic	EE25-13W-RI	13W-EE25	T1 See note 2)	1
99	Cement Resistor	KOA	BPR58CF10LJ	10mΩ/5W	R601, R602, R603, R604, R605, R606	6
100	Cement Resistor	KOA	BPR58CF22LK	22mΩ/5W	R607, R608, R609, R610, R611, R612	6
101	Capacitor	Jianghai	ECS2WKC821MLP350065	820uF/450V CD296 3000h Housing height 10mm 6.3mm pin length	E1, E2, E3, E4	4
102	Test Pin	KeyStone	5000 Red	TEST POINTS	TP1~TP30	30

Notes:

1) Remove the 6th pin in production

2) Custom made

9 References

Datasheets

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