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Effects of Oxidation on the Thermal Performance of DCB Power Modules

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Revision history

Date	Revision Level	Description	Page Number(s)
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1 Abstract

This application note proves that there is no thermal performance degradation by oxidation of the backside copper of a direct copper bonded (DCB) substrate.

2 Introduction

Power modules comprise a ceramic substrate for isolation and heat transfer with copper bonding on top and backside (DCB).

The backside of the DCB is forming a non-uniformly distributed thin layer of copper oxide (Cu_2O / CuO) due to the contact with air during manufacturing and storage. The visual appearance of such layers are red or pink for Cu_2O and black for CuO. High temperature and high humidity accelerate the formation of the oxide.

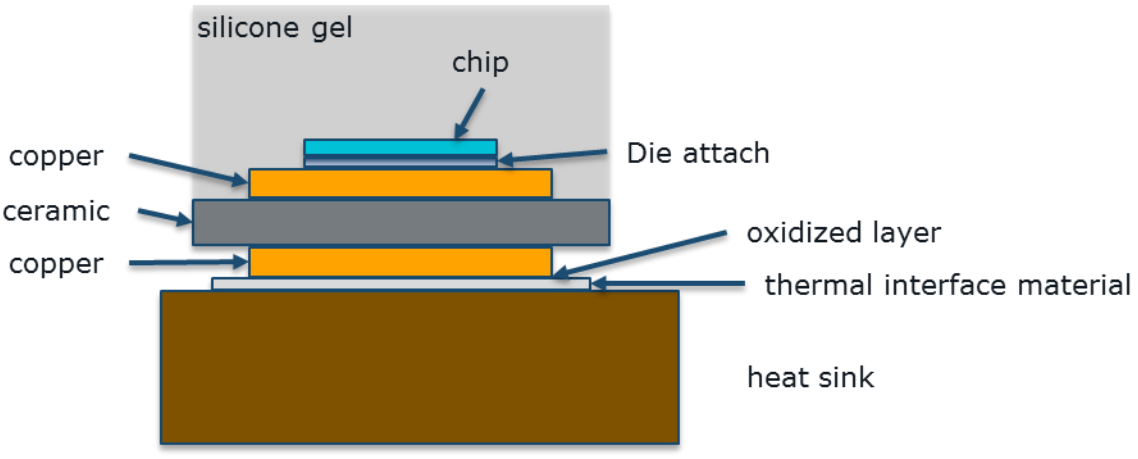


Figure 1: Thermal path cross-section of a power module

3 Thermal performance

This chapter investigates the thermal resistance (R_{th}) from chip junction to heat sink and additionally per layer. It will be proven that the oxide layer is not degrading the thermal performance of the power module.

3.1 Rth measurements of different oxidized samples

Four samples with different levels of oxidation and one sample without oxidation were compared in terms of $R_{th(j-s)}$.

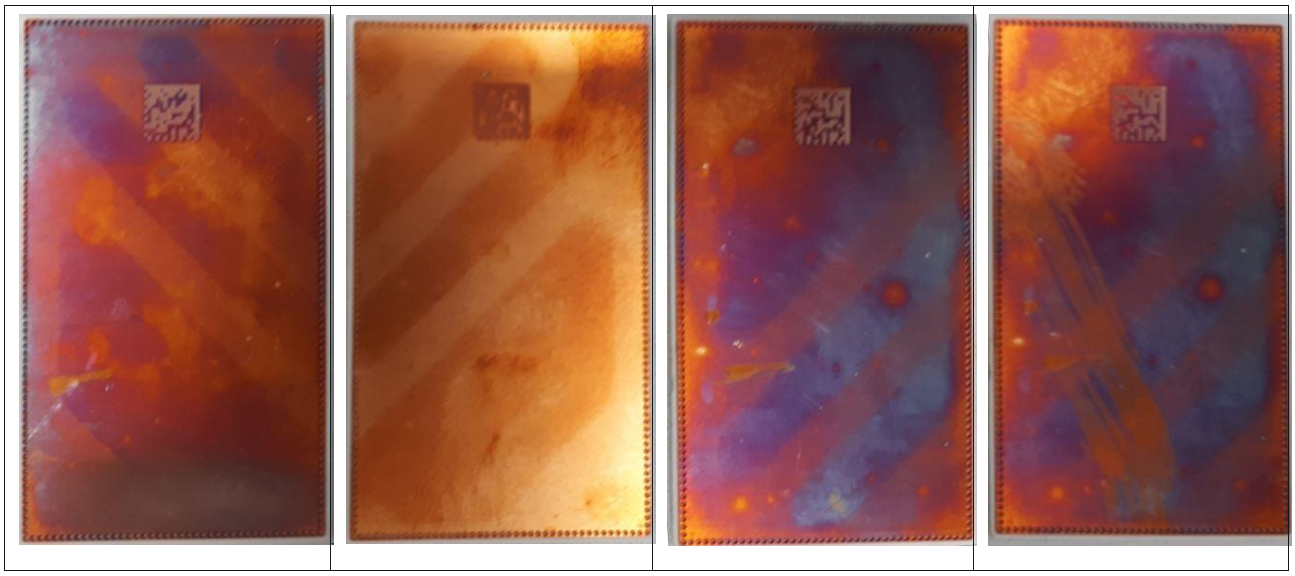
	Pure copper surface (no oxidation) Measured thermal resistance: $R_{th(j-s)}$ = 1,05 K/W (reference value)
	Highest oxidation level Measured thermal resistance: $R_{th(j-s)}$ = 1,06 K/W (+1% to reference)
	High oxidation level Measured thermal resistance: $R_{th(j-s)}$ = 1,04 K/W (-1% to reference)
	Slight oxidation Measured thermal resistance: $R_{th(j-s)}$ = 1,03 K/W (-2% to reference)
	Local surface imperfections Measured thermal resistance: $R_{th(j-s)}$ = 1,04 K/W (-1% to reference)

Figure 2: caption (change according to picture)

Above comparison shows no significant difference in measured $R_{th(j-s)}$ of differently oxidized module samples. The difference between measurements is well within the measurement accuracy.

3.2 Other possible surface appearance

In addition to the above described full oxidation of the DCB backside surface, also partial oxidation or oxidation with different grade can occur. Following pictures show the typical appearance.



3.3 Rth distribution per layer

Knowing the heat generating area and thickness, thermal conductivity and spreading of each layer, the thermal resistance of each thermally conducting layer can be analytically determined.

layer	Rth [K/W]	contribution [%]
chip	0.033	3.22
solder	0.075	7.34
top copper	0.022	2.12
ceramic	0.484	47.16
bottom copper	0.013	1.25
oxidized layer (100 nm)	0.00016	0.02
PC-TIM	0.399	38.89
SUM	1.026	100

Table 1: Calculated Rth distribution per layer

The contribution of the 100 nm thick oxidized copper layer to the overall thermal resistance is very small (0.02%). The ceramic and the thermal interface material (TIM) dominate the thermal resistance, which are 3000 respectively 2400 times higher than the copper oxide layer thermal resistance.

3.4 Thermal spreading

The thermal spreading is analyzed with FEM simulation of the two dimensional power module stack up.

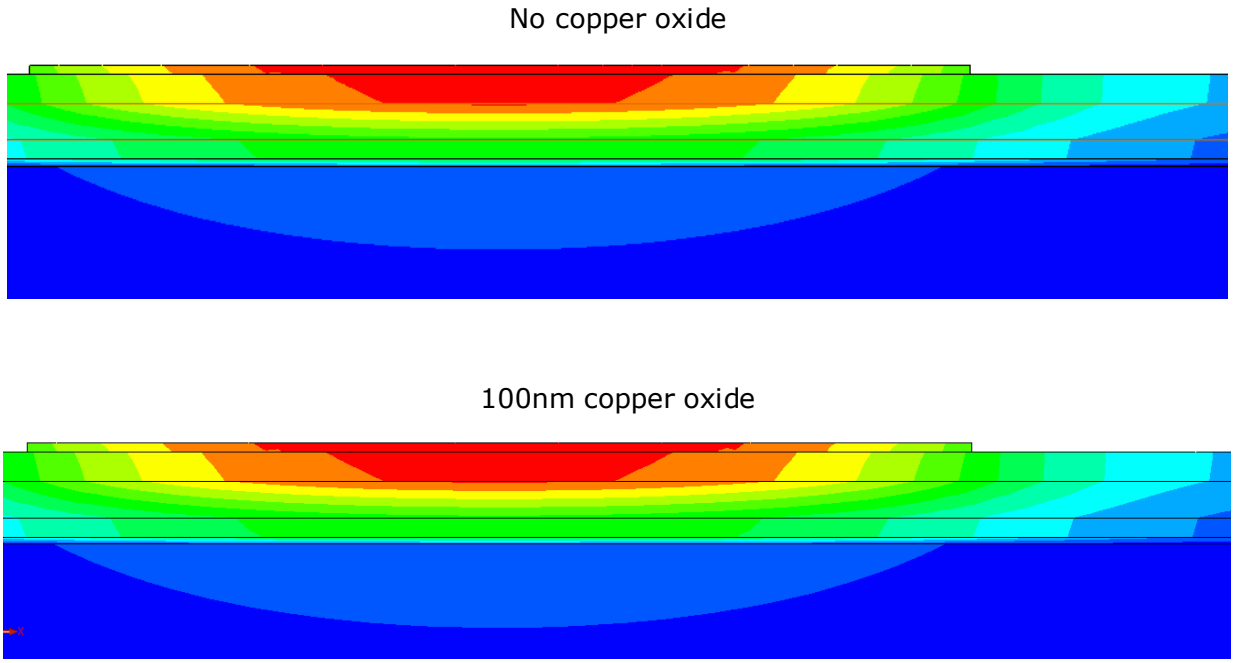


Figure 3: Simulation of heat spreading without copper oxide and with 100nm copper oxide layer

Above simulation results show no noticeable difference in the thermal spreading between non-oxidized and oxidized layer.

4 Conclusion

Measurement, calculation and simulation show that the very thin oxidized copper layer has negligible influence on the thermal resistance between chip and heat sink and thus on the thermal performance of the power module.